New electronics for ALICE FIT detector.

Towards grant proposal

18.07.2022

ALICE detector (Courtesy: CERN)

CERN Council responds to Russian invasion of Ukraine

News | At CERN | 08 March, 2022

- CERN will not engage in new collaborations with the Russian Federation and its institutions until further notice

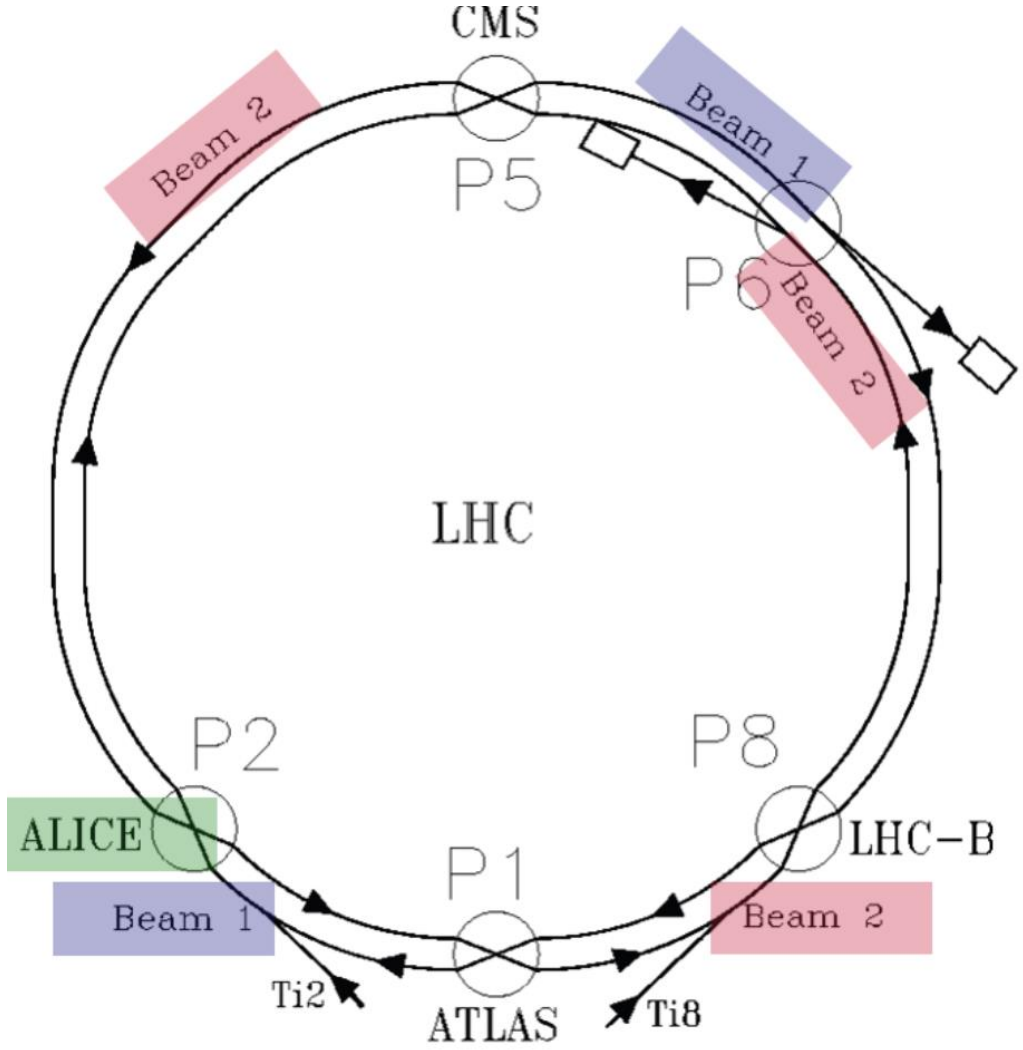
CERN Council declares its intention to terminate cooperation agreements with Russia and Belarus at their expiration dates in 2024

News | At CERN | 17 June, 2022

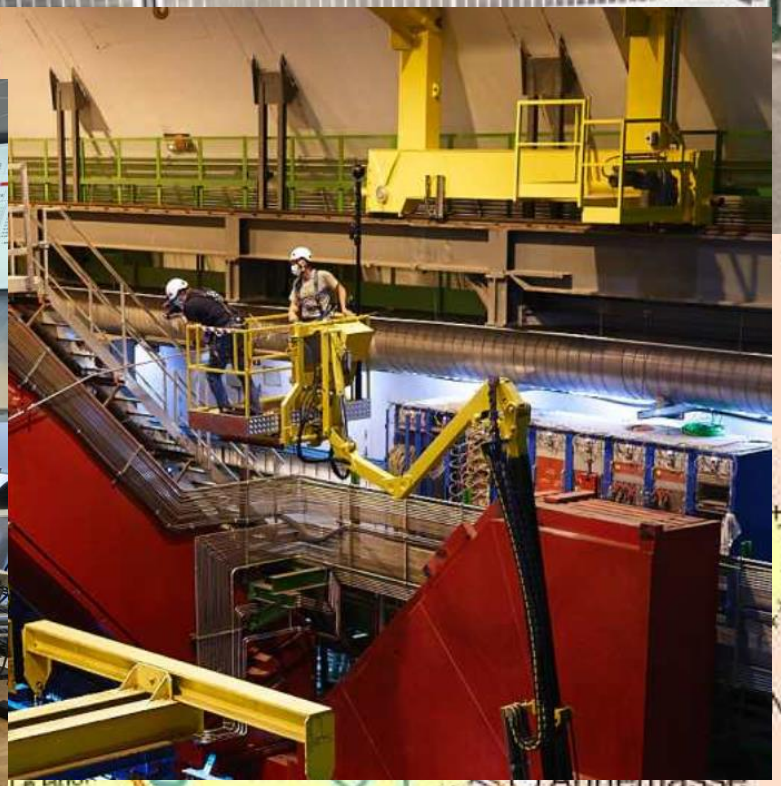
- The ICA with the Russian Federation expires in December 2024, that with the Republic of Belarus in June 2024
- decision allows such researchers to continue their scientific work at CERN until the current agreements expire and to plan for their future.

LHC accelerator in CERN

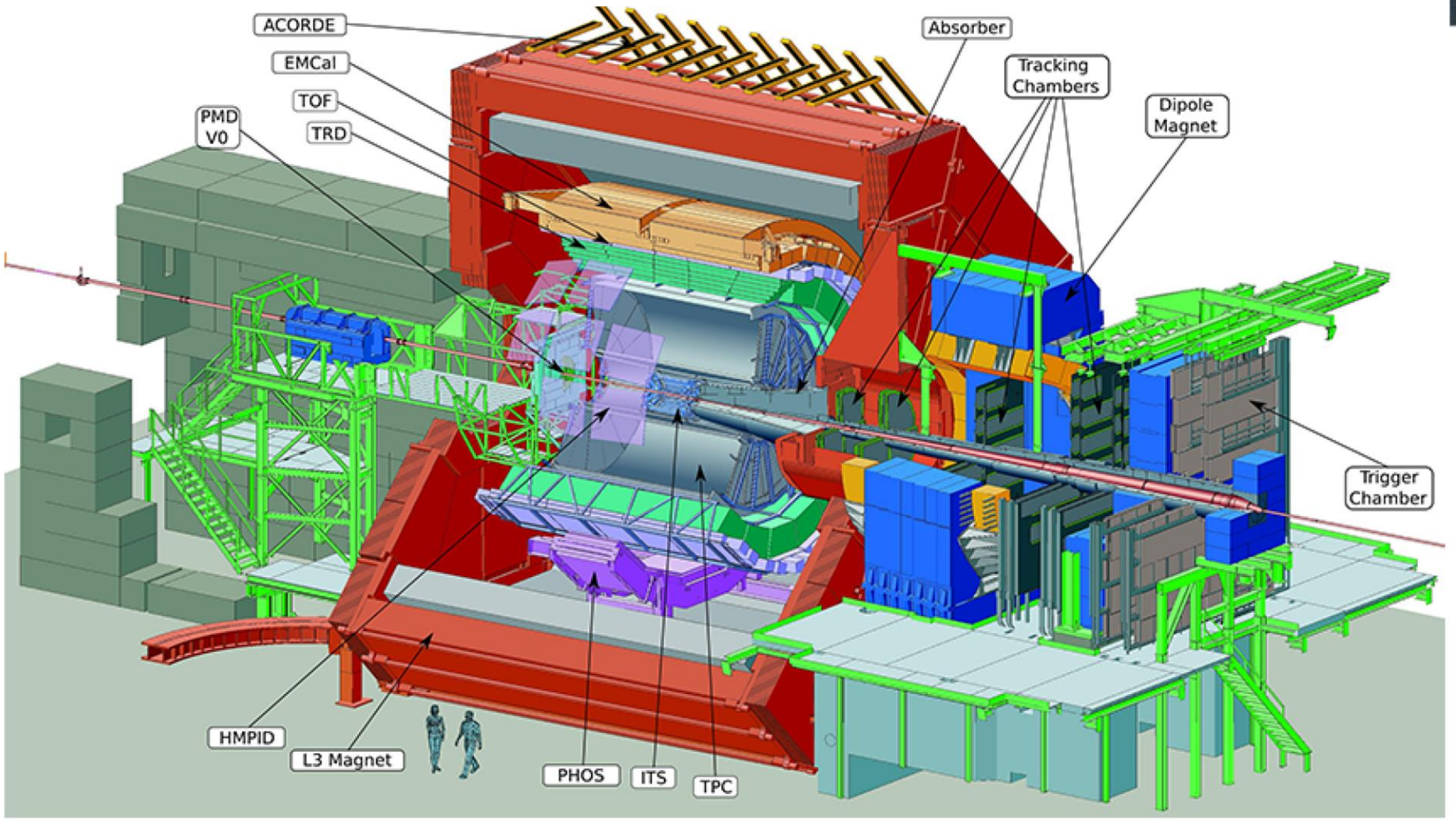
- Particles are injected in bunches into two rings
- Selected bunches collide at the interaction points (IP1, IP2, IP5, IP8)
- ALICE – A Large Ion Collider Experiment
- ALICE experimant is located at IP2, near Beam 1 injection point



ALICE – Point 2

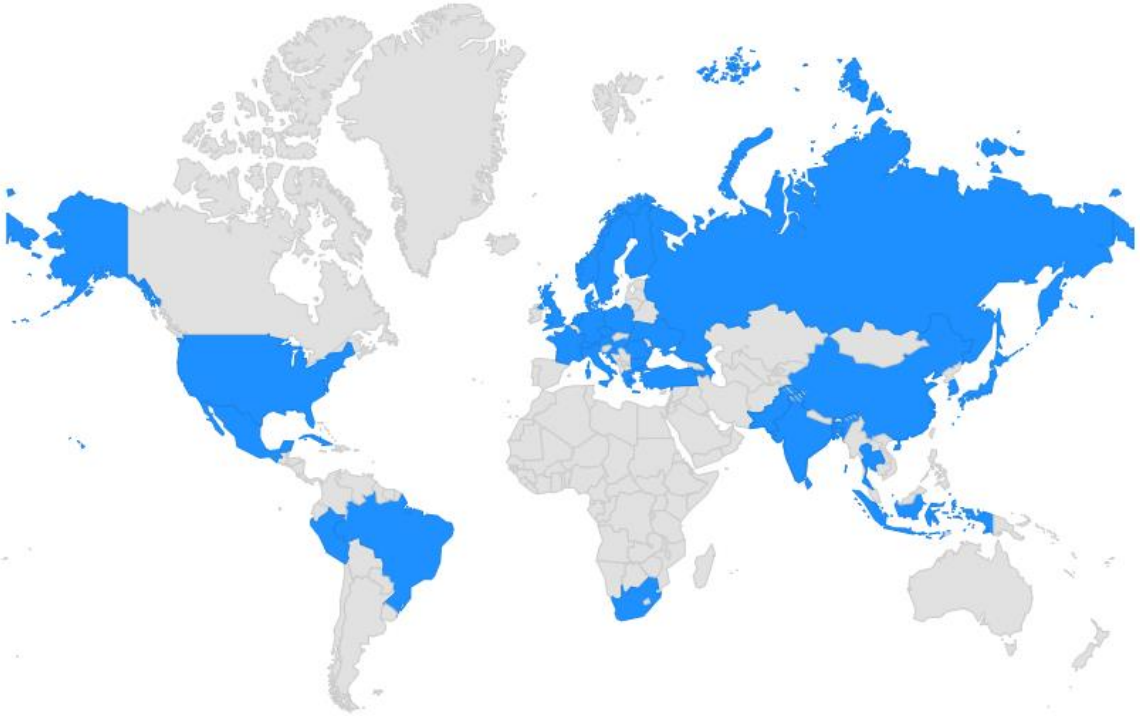


ALICE multi-detector



ALICE collaboration

- ALICE collaboration:
  - 40 countries, 173 institutes, 2046 members



- ALICE-PL
  - National Centre for Nuclear Research, Warsa
  - Warsaw University of Technology, Warsaw
  - The Henryk Niewodniczanski Institute of Nuc
  - AGH University of Science and Technology, K

ALICE-AGH (full member since 2020)

Instytut Elektroniki

Instytut Informatyki

Katedra Automatyki
i Robotyki

Member		Category
Bartosz BALIS	M&O	Senior Engineer
Roman Jan DEBSKI	M&O	Senior Engineer
Marek Boguslaw GORGON	M&O	Senior Engineer
Adrian HORZYK	M&O	Senior Engineer
Miroslaw JABLONSKI	M&O	Senior Engineer
Jacek Pawel KITOWSKI	M&O	Senior Engineer
Pawel Grzegorz RUSSEK	M&O	Senior Engineer
Sebastian Dominik KORYCIAK		PhD Student

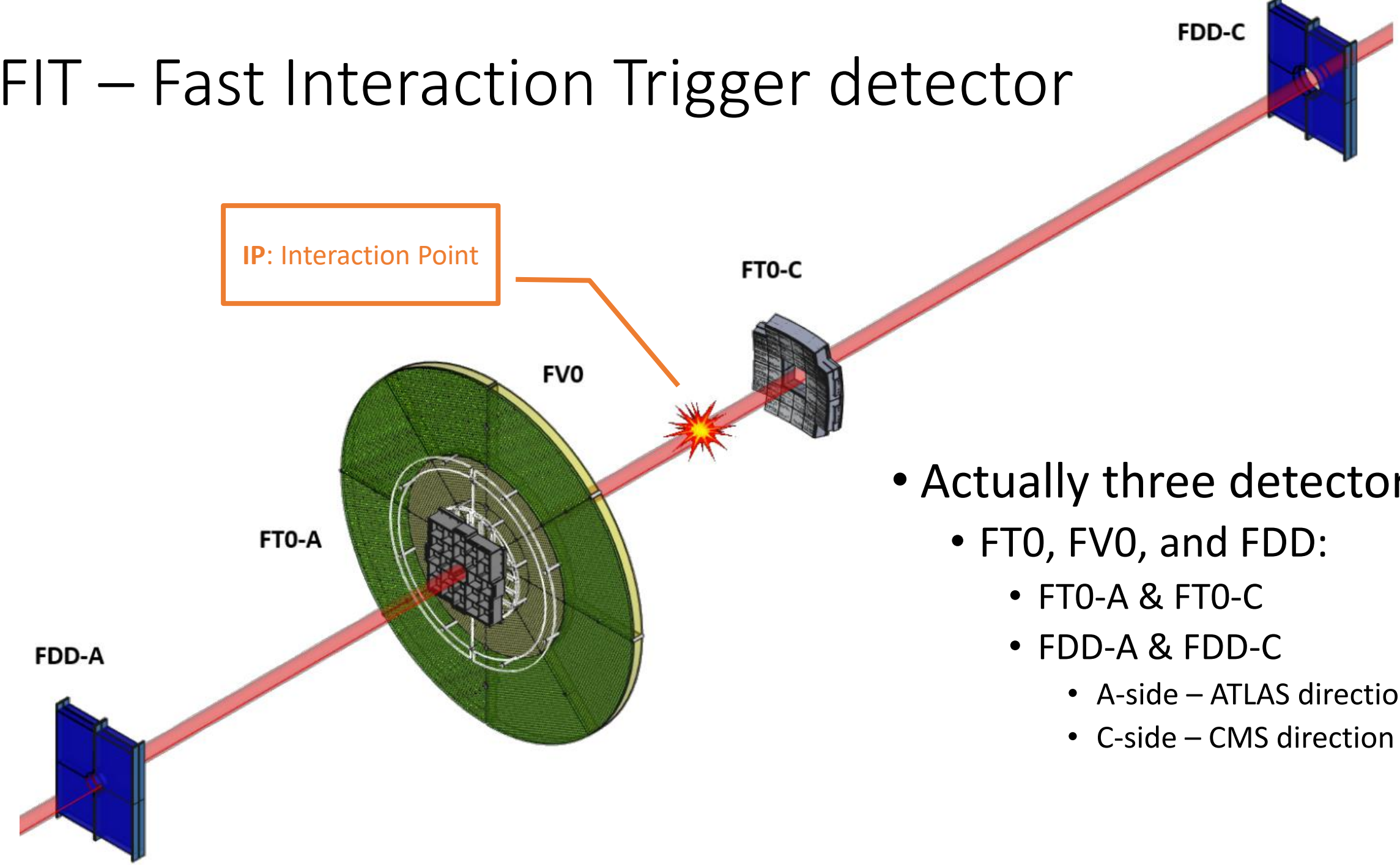
O2, CCDB

ML-based anomalies detection

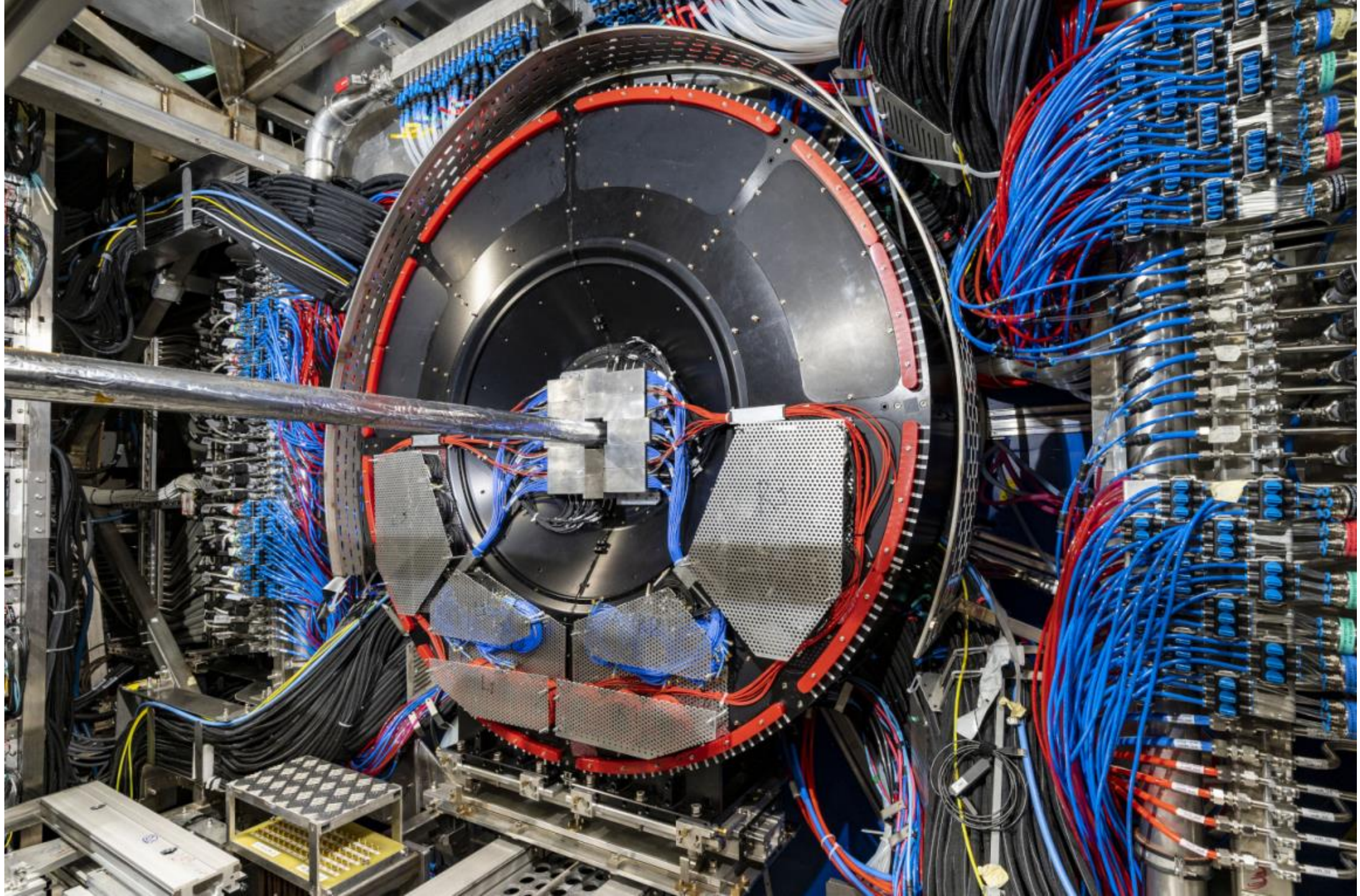
Team Lider
O2, CCDB

Firmware for FPGA
Trigger for FIT

FIT – Fast Interaction Trigger detector



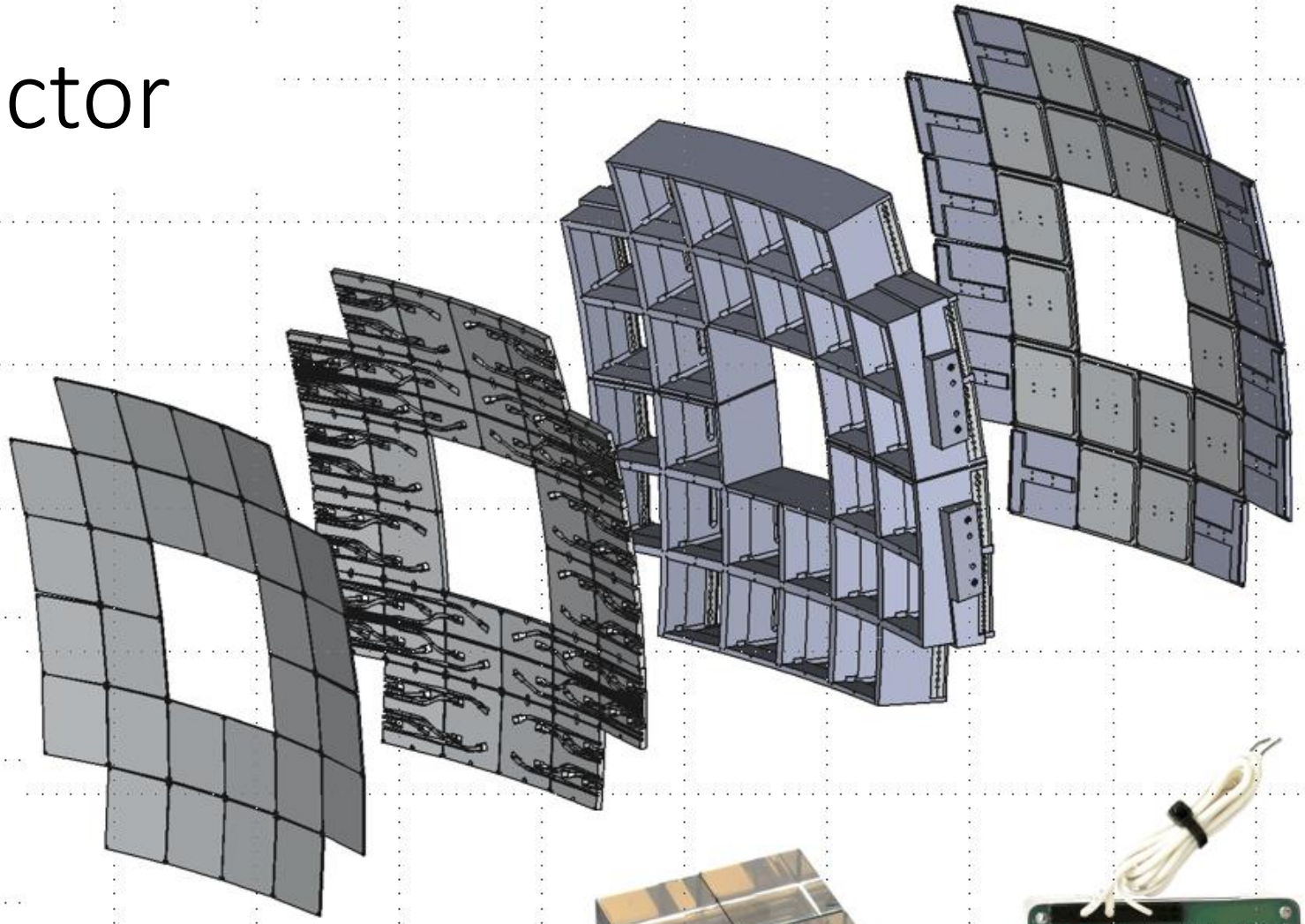
- Actually three detectors:
  - FT0, FV0, and FDD:
    - FT0-A & FT0-C
    - FDD-A & FDD-C
      - A-side – ATLAS direction
      - C-side – CMS direction

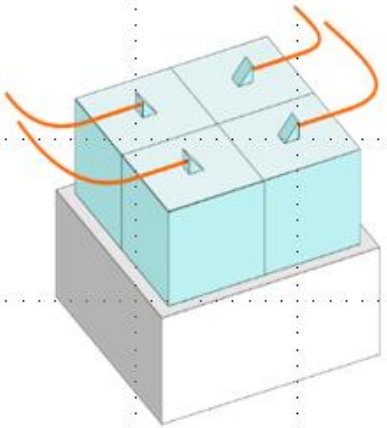


FIT project

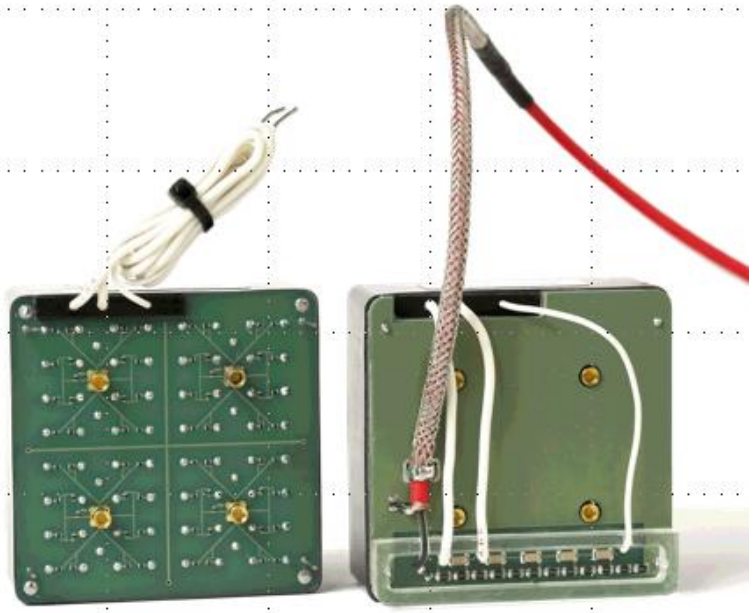
- FIT Project members:
  - Project Lider: Władysław Trzaska (Jyvaskyla, Finland)
  - Members: Austria, Czech Republic, Denmark, Finland, Mexico, Poland, **Russia**, USA
- FIT Trigger coordinator: Jacek Otwinowski, Krakow
- Institute of Nuclear Research (INR), Moscow
  - Hardware
    - Readout electronics
      - Full design, Production, Testing&Calibration, Maintenance and Upgrade
      - FPGA firmware design
    - Laser Calibration System and optical fibres
  - Software
    - Detector Control System (SCADA)
    - O2 cluster system – Software First Level Processors
  - On-call experts

FT0 detector

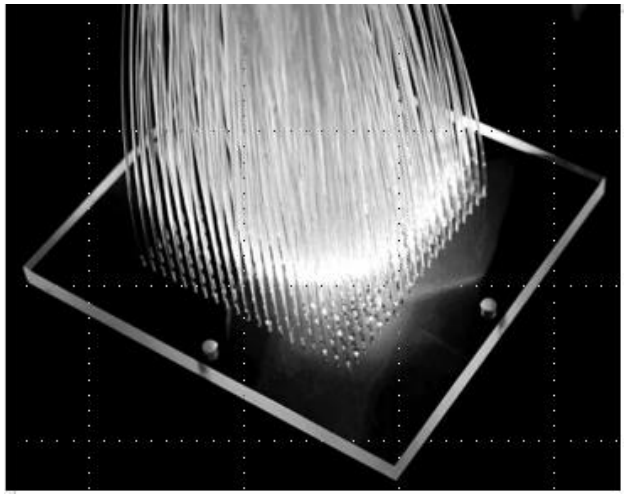




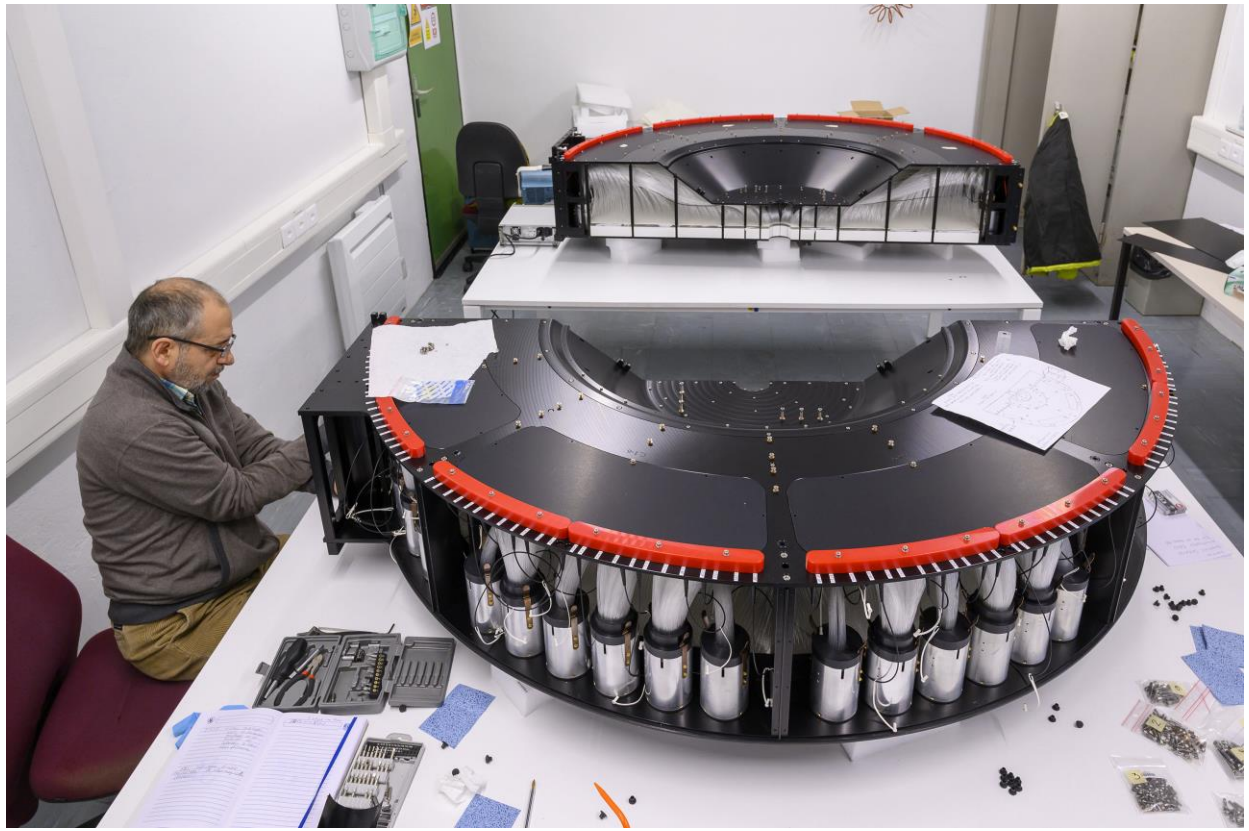
- 2 cm thick quartz radiators
- Modified XP85012 MCP/PMT
- 1 MIP resolution → 20 ps



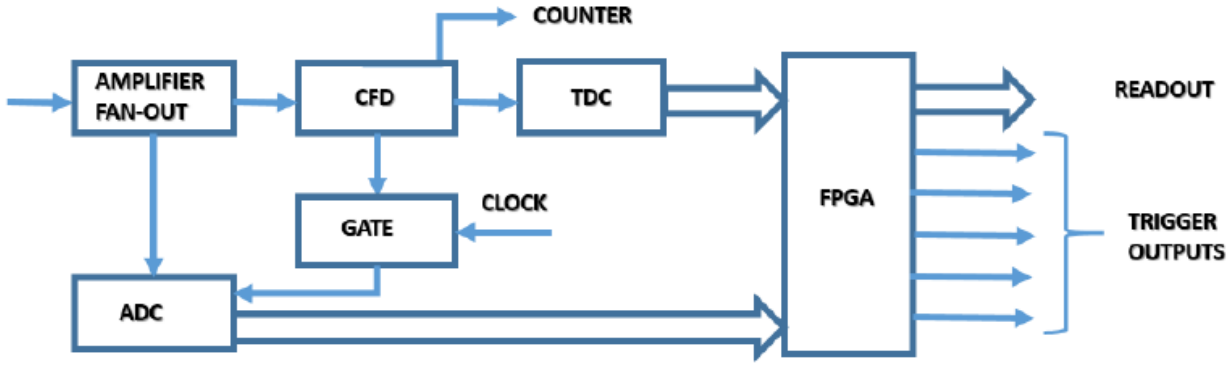
FV0 detector: sciltillator ring

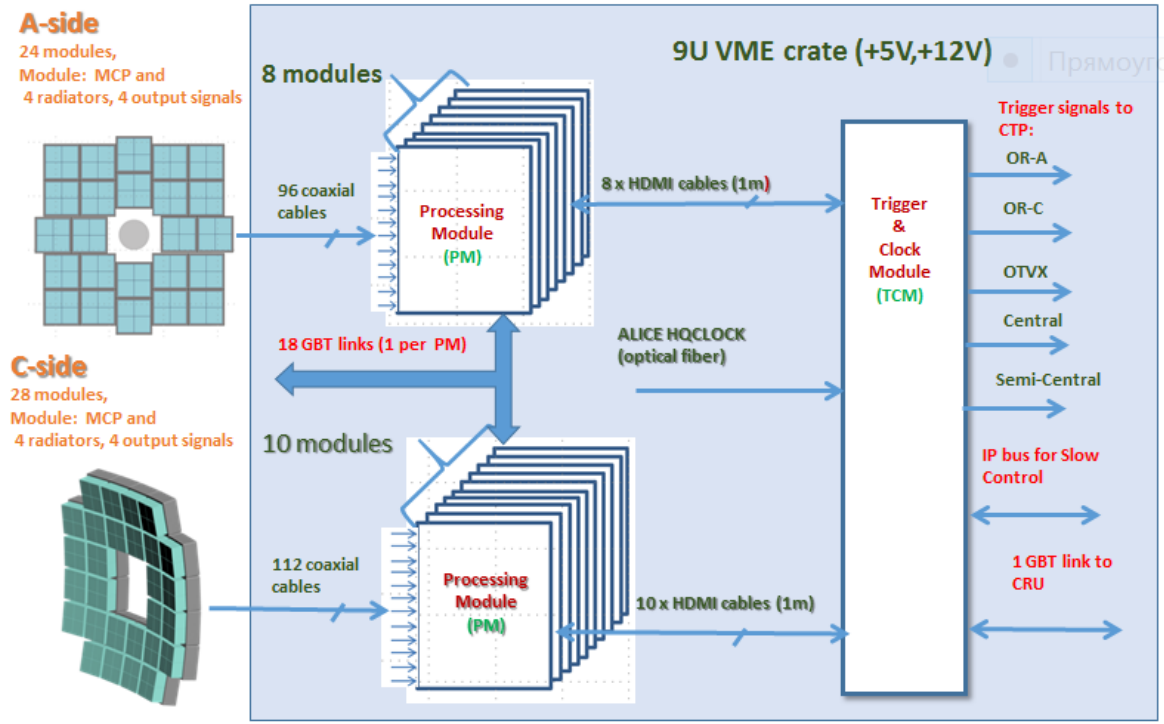


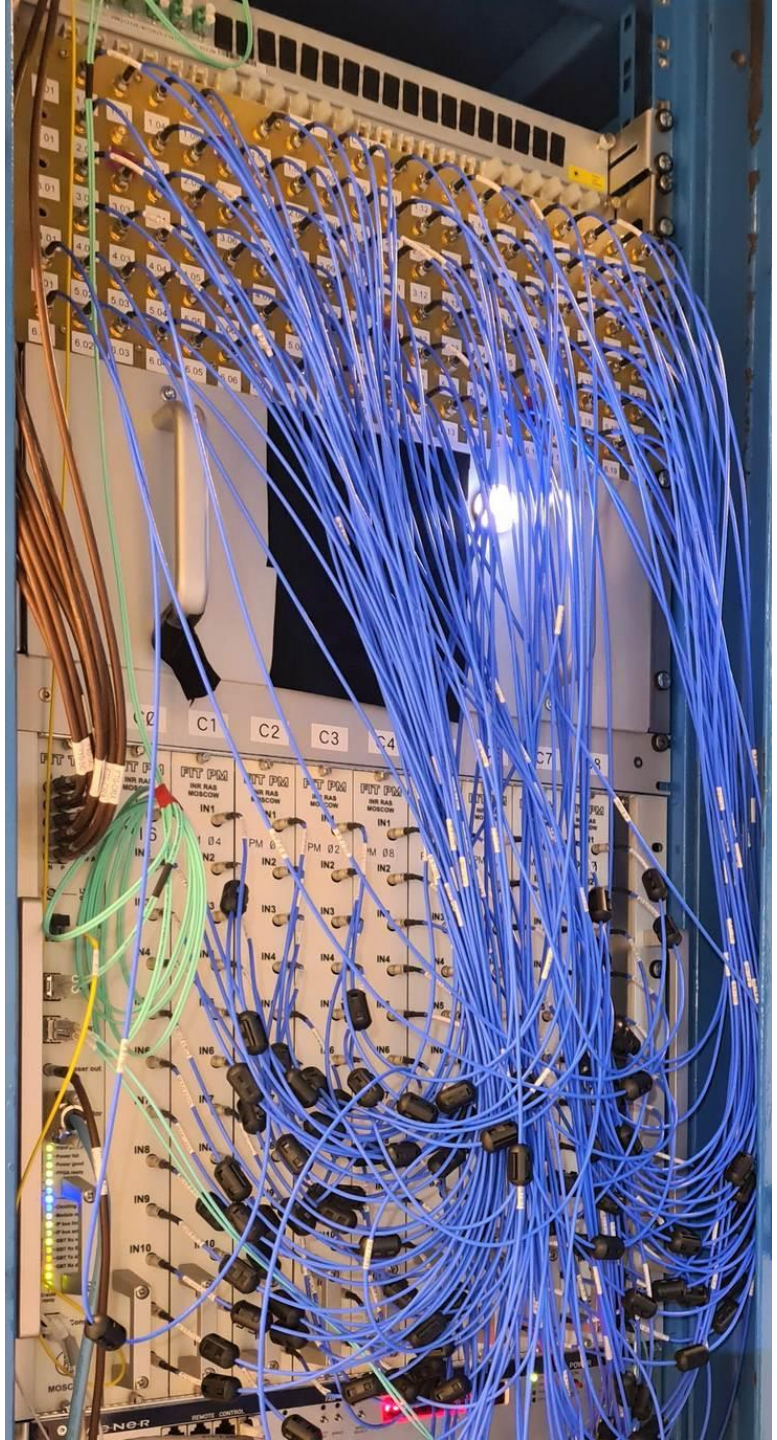
- 4 cm thick EJ-204 scint.
- Clear Asahi fibre
- H6614-70-Y001 PMT
- 1 MIP → 200-250 ps



Readout electronics

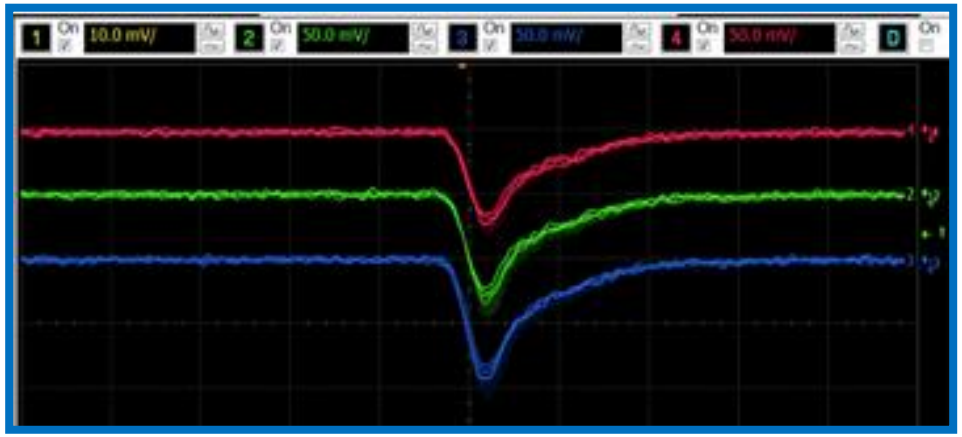






Signal properties from detector for FIT electronics

T0+

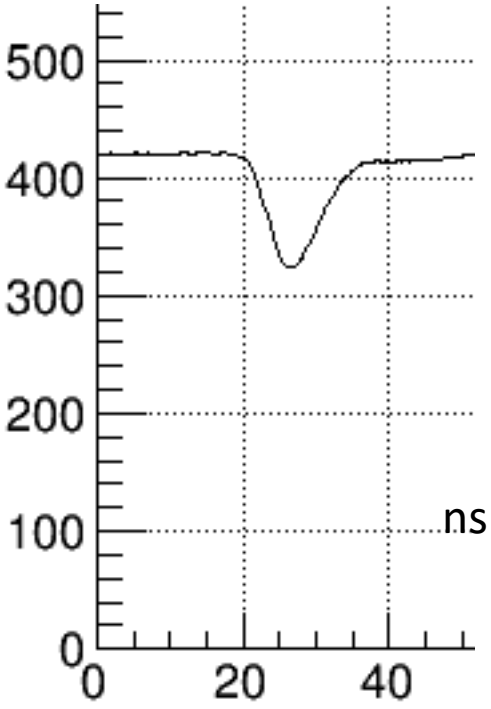


5 ns / div

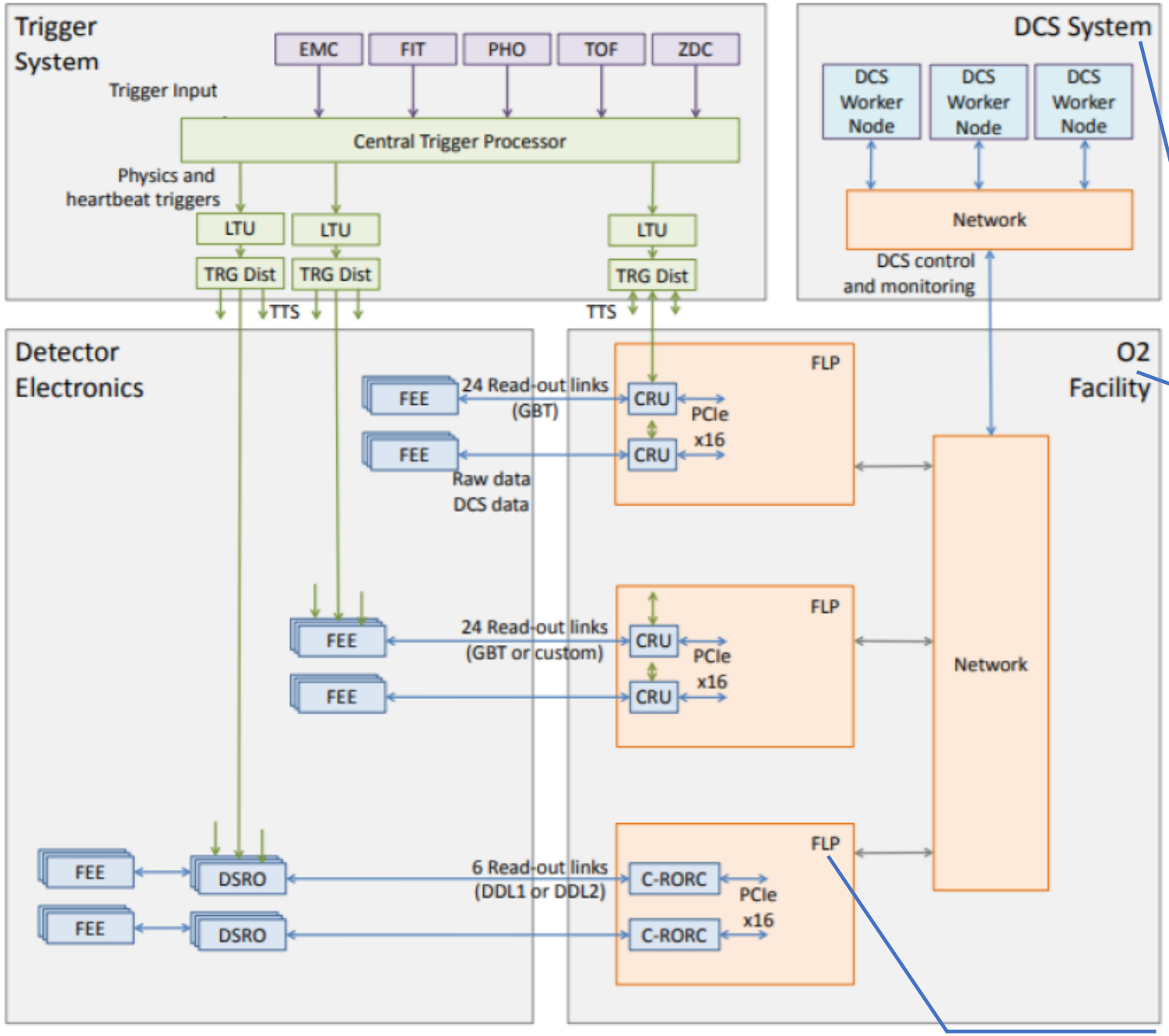
For FIT T0+ & FIT V0+

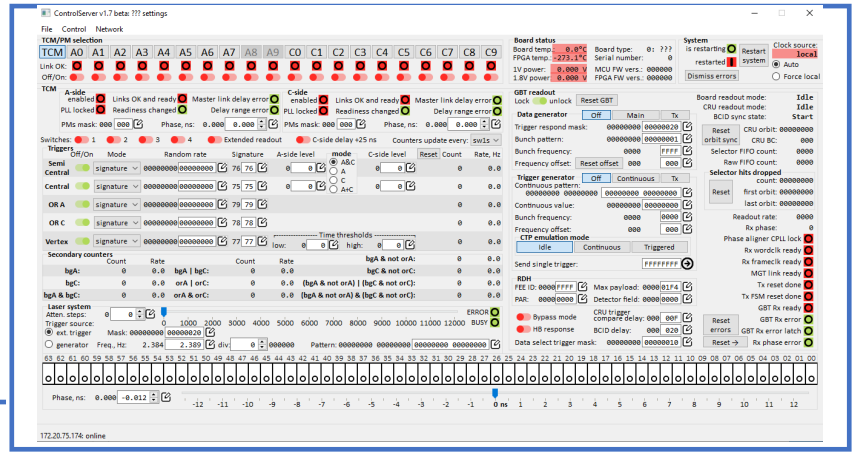
PMT gain adjusted for 1 MIP pulse = 7.5 mV at the FEE inputs.
Max. rate = 2 MHz

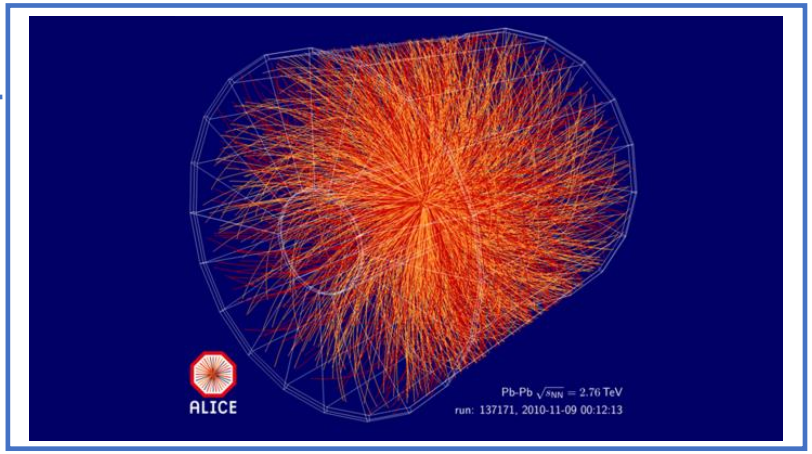
V0+



T0+ MCP PMT signal parameters at module inputs Thick cables	Pulse amplitudes 3mV – 2000 mV • Leading edge ~1.6 ns, • Trailing edge ~4 ns
V0+ Fine mesh PMT parameters at module inputs Standard cables	Pulse amplitudes 3mV – 5000 mV, • Leading edge ~5-6 ns, • Trailing edge ~11-12 ns


Trigger System
Trigger Input
EMC
FIT
PHO
TOF
ZDC
Central Trigger Processor
Physics and heartbeat triggers
LTU
LTU
LTU
TRG Dist
TRG Dist
TRG Dist
TTS
TTS
DCS System
DCS Worker Node
DCS Worker Node
DCS Worker Node
Network
DCS control and monitoring
Detector Electronics
O2 Facility
FEE
24 Read-out links (GBT)
CRU
PCIe x16
FLP
Raw data
DCS data
24 Read-out links (GBT or custom)
Network
DSRO
6 Read-out links (DDL1 or DDL2)
C-RORC
PCIe x16




ALICE
Pb-Pb $\sqrt{s_{NN}}$ = 2.76 TeV
run: 137171, 2010-11-09 00:12:13

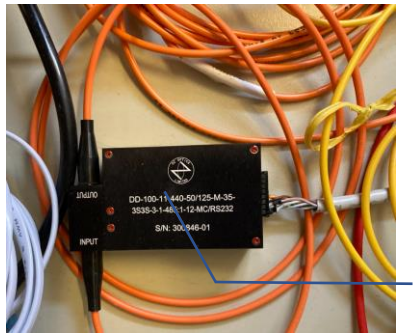

CPPM

FIT laboratory

TCM

4×PM

LASER



LASER CONTROLER

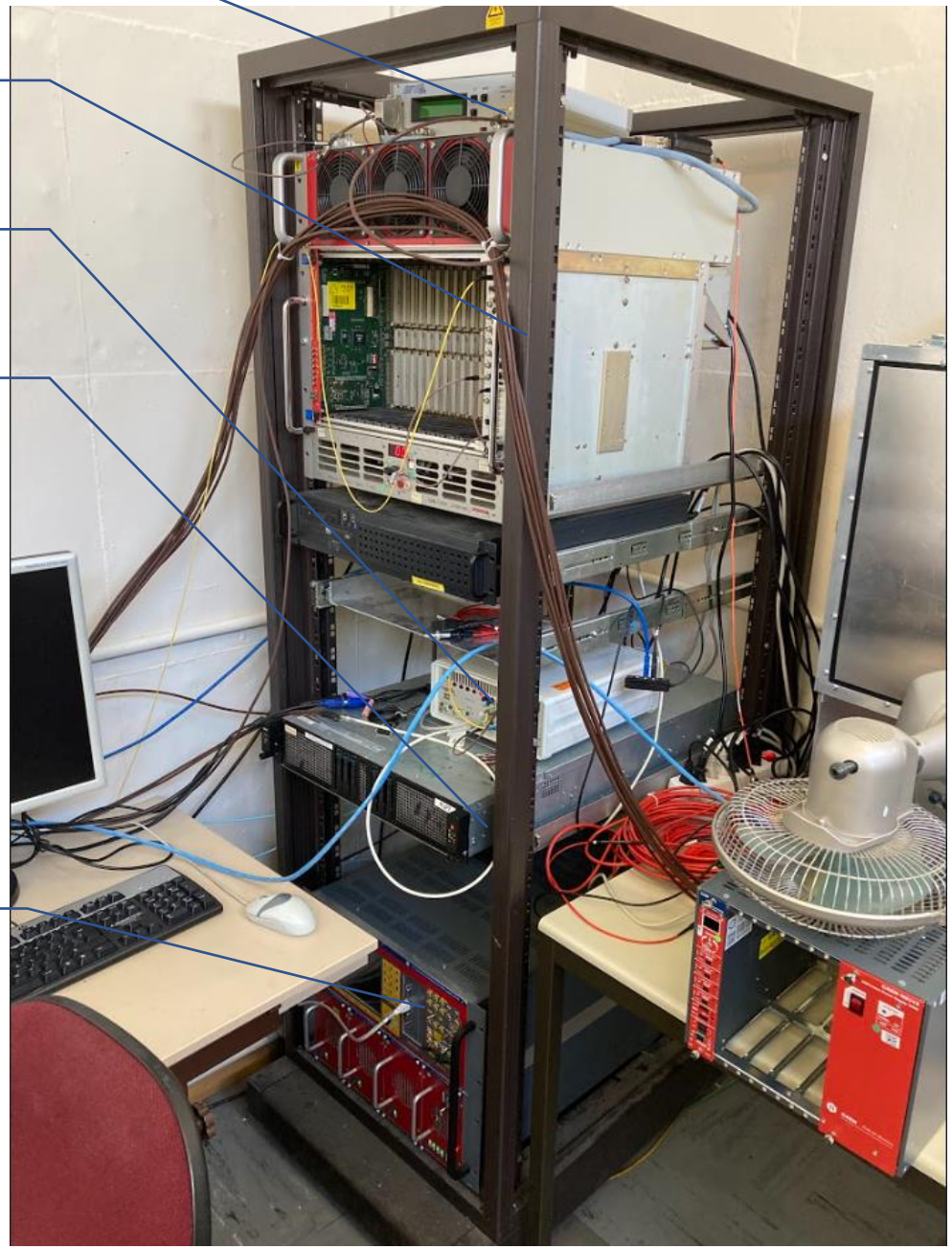
LHC CLOCK GEN.

LTU

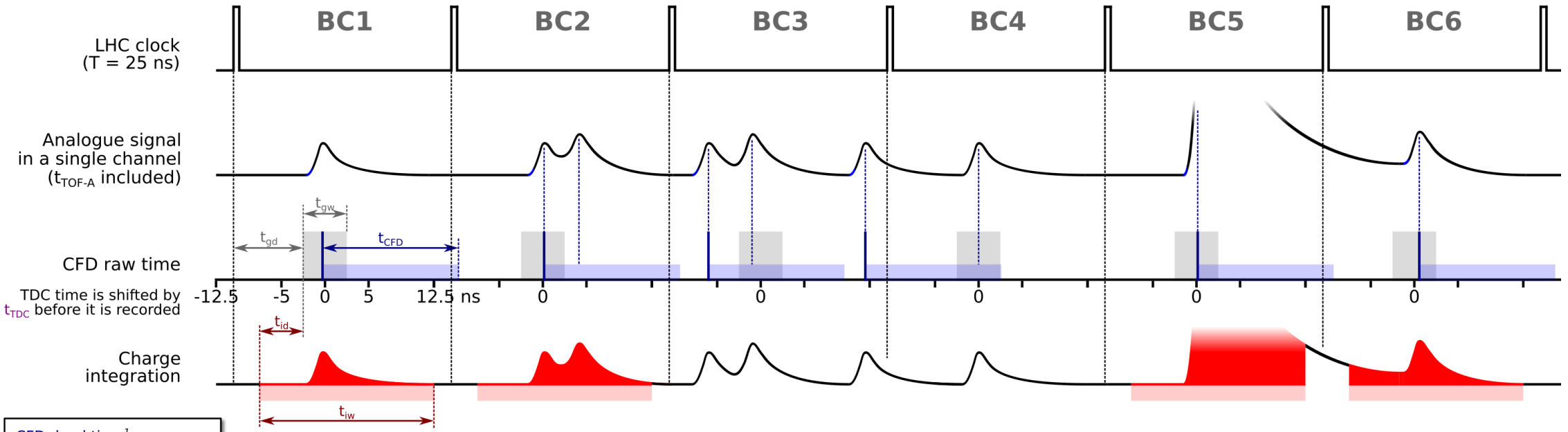
FLP+CRU

HV POWER

ATTENUATOR



Readout timings



CFD dead time[1]:
t_{CFD} = 15..16 ns

Gate width:
A: t_{gw} = 5 ns

Gate delay[2]:
A: t_{gd} ≅ 7.5 ns
C: t_{gd} ≅ -0.1 ns

Integration window width:
t_{iw} = 19..20 ns

Integration window delay[2]:
t_{id} = -3.5 ns

TDC time shift:
$t_{TDC} = t_{gd} + t_{gw} / 2$

Time-of-flight
A: t_{TOF} ≅ 10 ns
C: t_{TOF} ≅ 2.4 ns

Single hit at the interaction time

CFD is triggered by sufficiently steep leading edge

CFD time is within ± 2.5 ns gate, so the charge integration is triggered

Time and charge is recorded

Two hits within the CFD dead time, second hit comes from background

CFD records only time of the first hit

Charge from both hits is integrated

Reconstructed multiplicity contains background contamination

Time and charge is recorded

Three hits: initial 2 are within CFD dead time, first and third hit comes from background

CFD is triggered by the first pulse, but integrator does not start because the pulse is outside of ± 2.5 ns gate

The second pulse is lost - neither its time nor charge is recorded

The third pulse triggers CFD, but not integrator

2 time values are recorded and pile-up flag is set

Single hit after background hit, that occured late in the previous BC

Otherwise valid hit is lost, because the CFD was still busy processing previous background hit

No data is recorded

Many hits

Collected charge is slightly underestimated because tail is lost

Timiing may be inaccurate if CFD was saturated

Time and charge is recorded

Single hit after high-charge event

Signal level has not dropped to the base level, because of the tail of preceeding hit

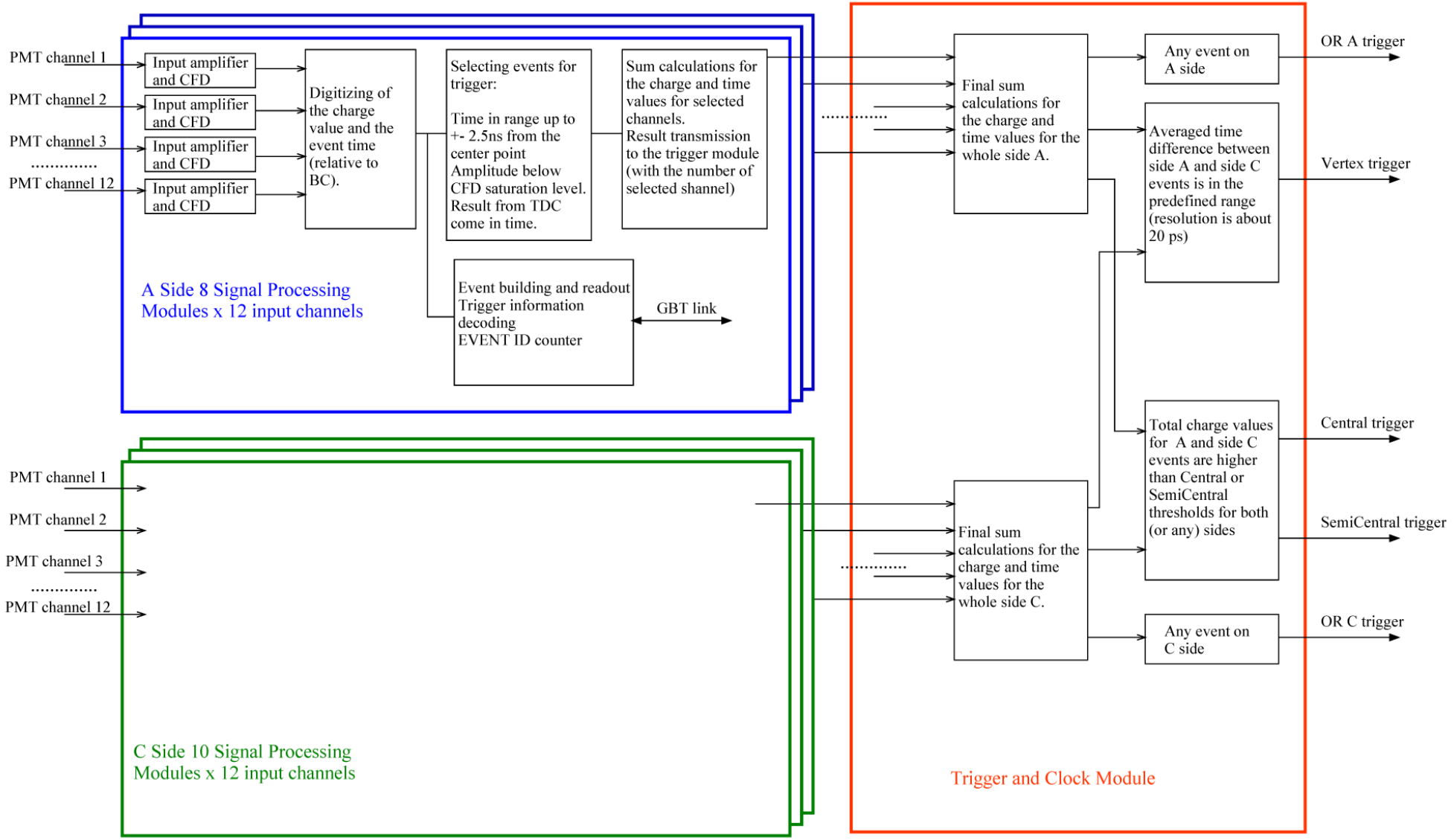
CFD triggers, but time is slightly shifted and charge contains a portion of tail from the previous BC

Time and charge is recorded

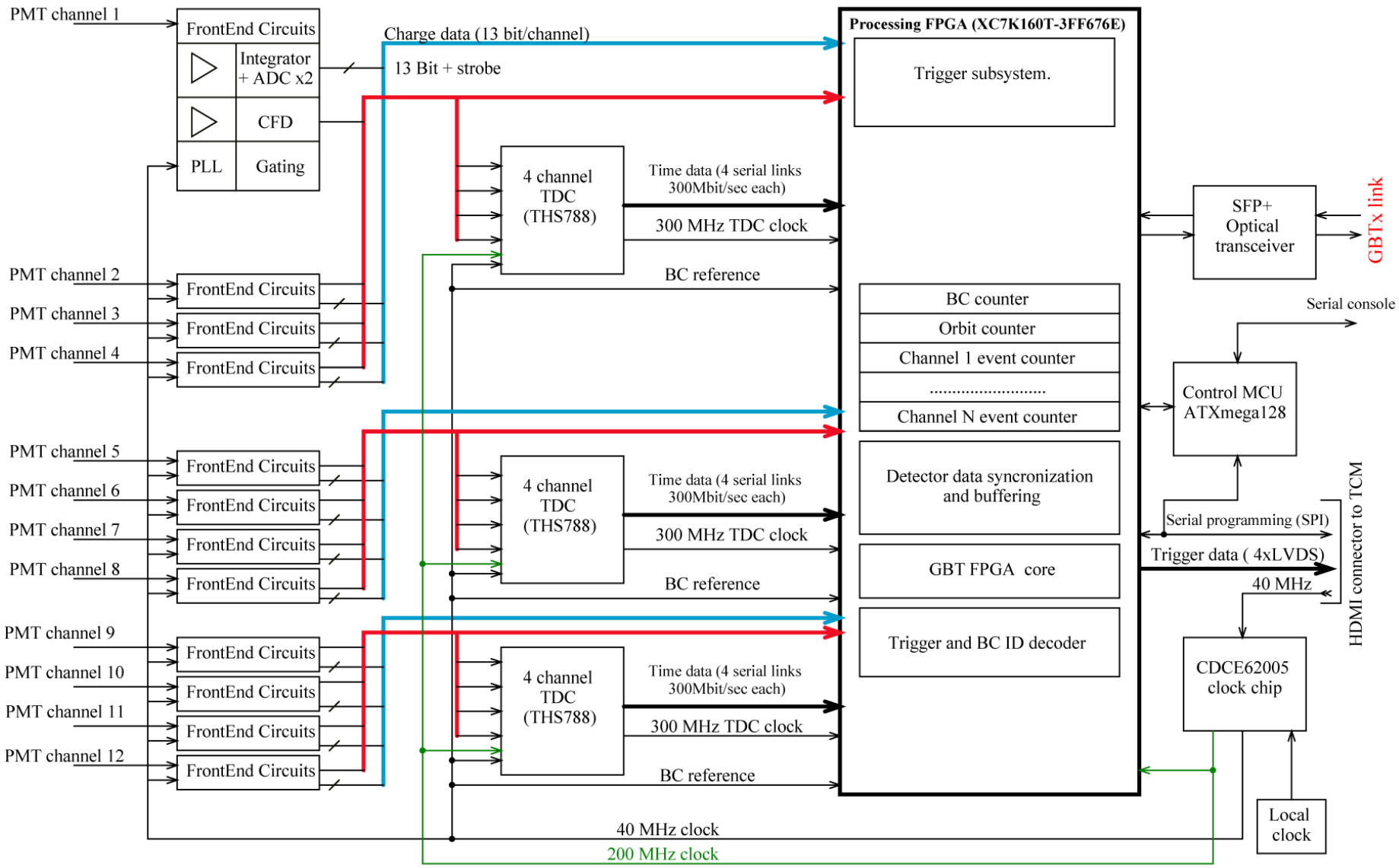
[1] *Dead time may depend on channel*

[2] *Delays are adjustable individually for each channel via PM registers*

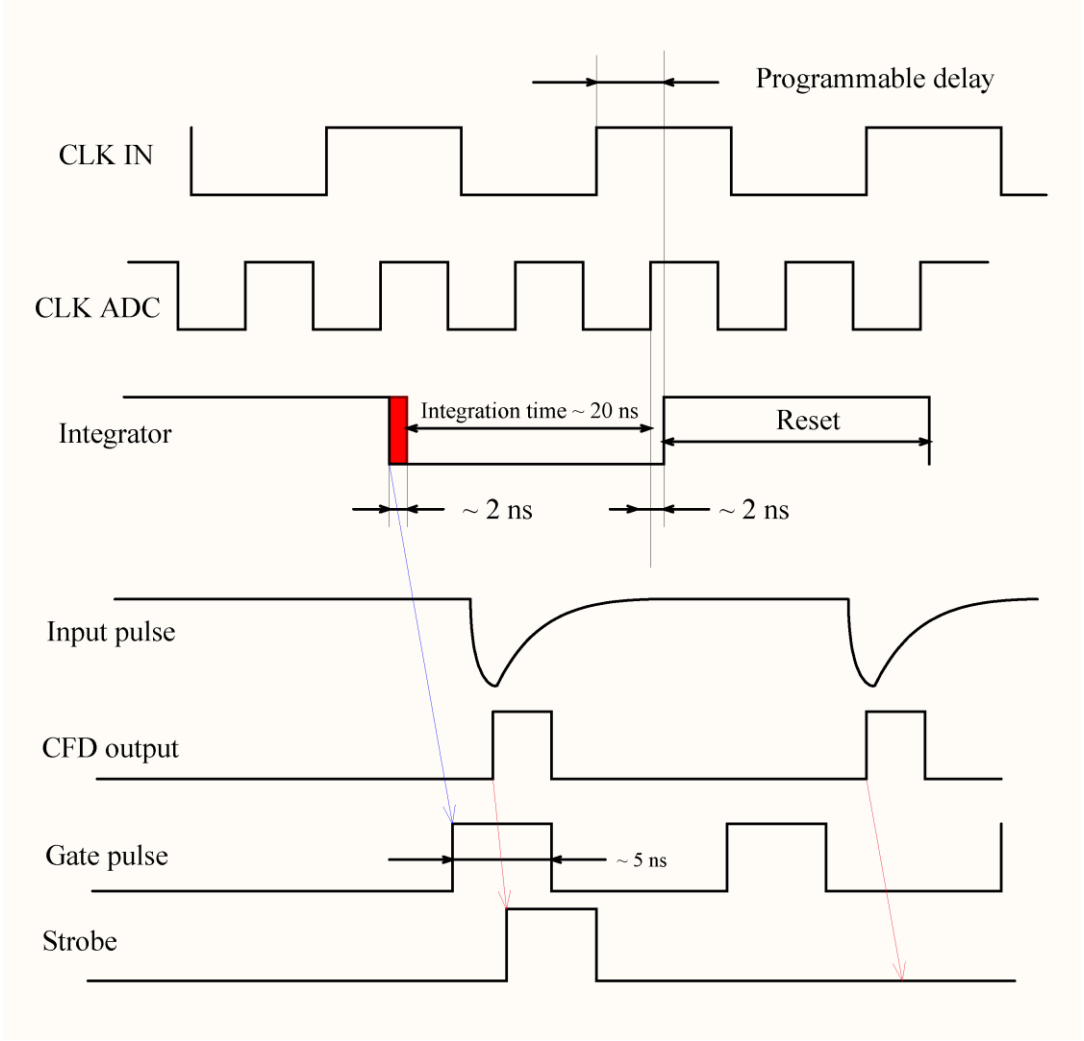
Readout electronics structure

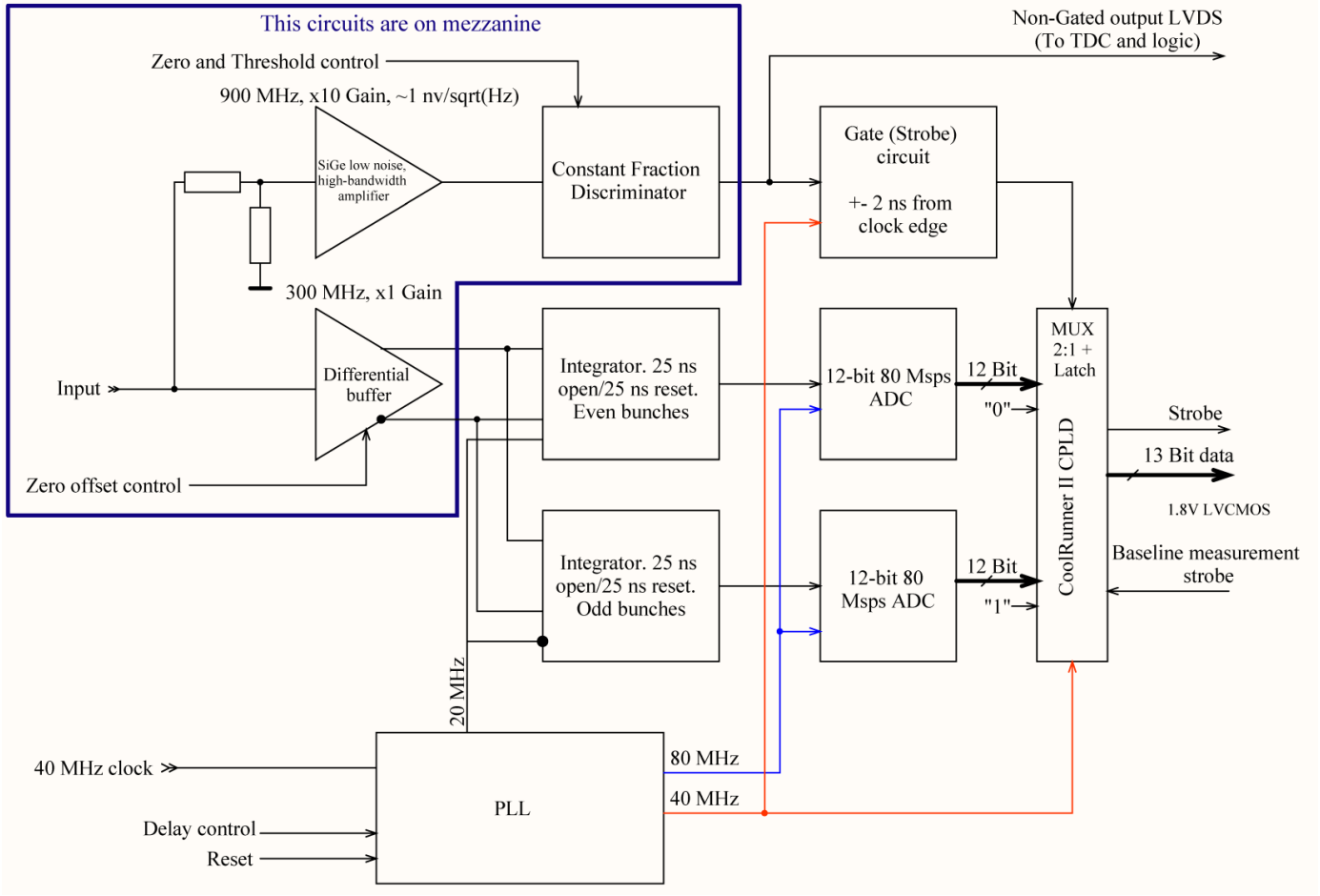


Processing Module (PM) structure

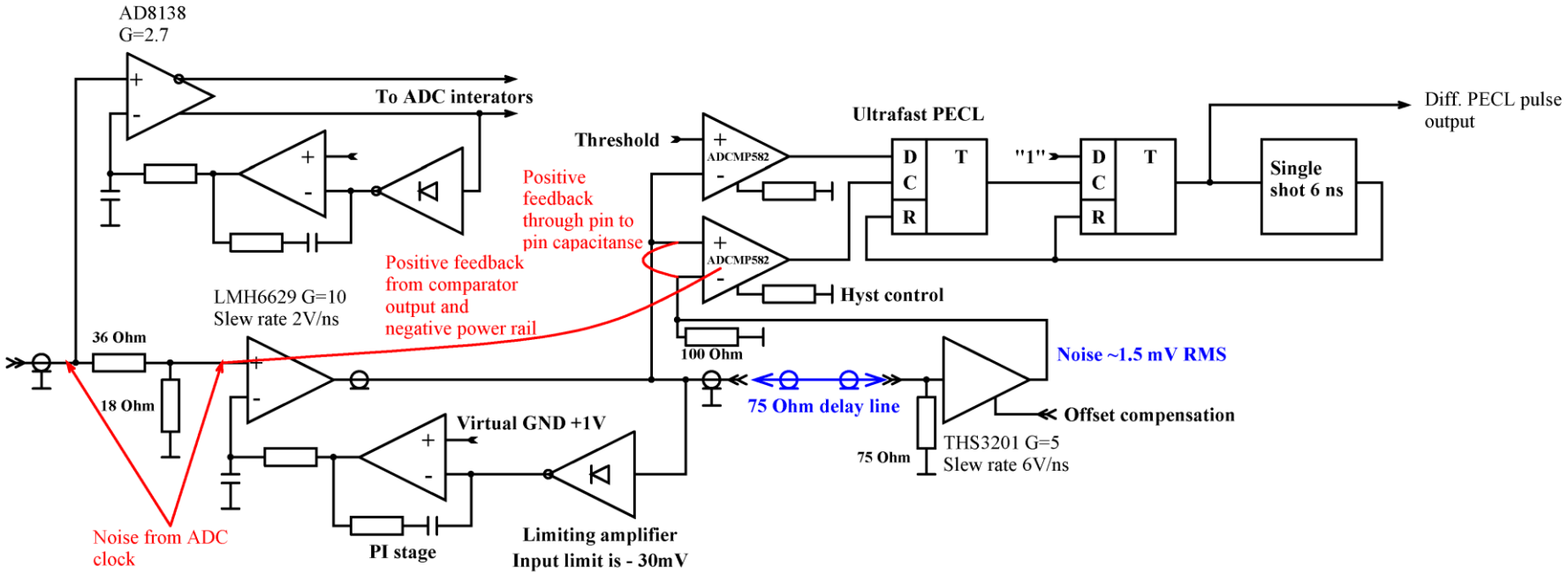


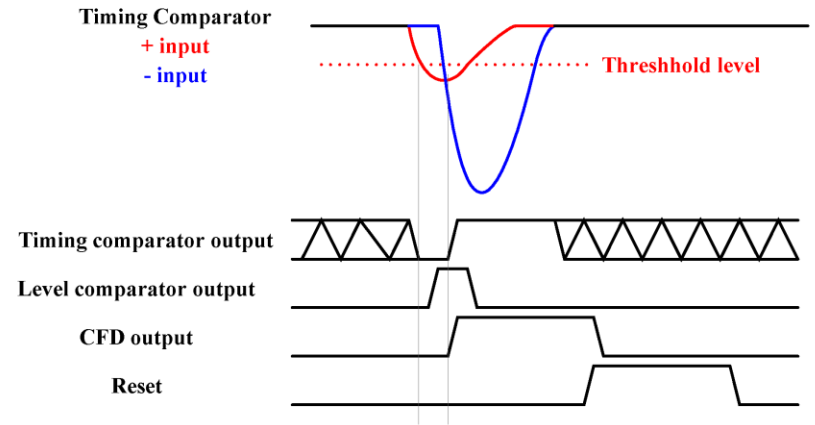
PM analog front end electronics

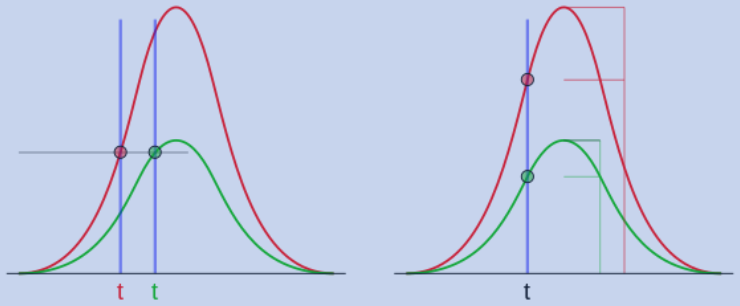




Constant Fraction Discriminator (CFD)

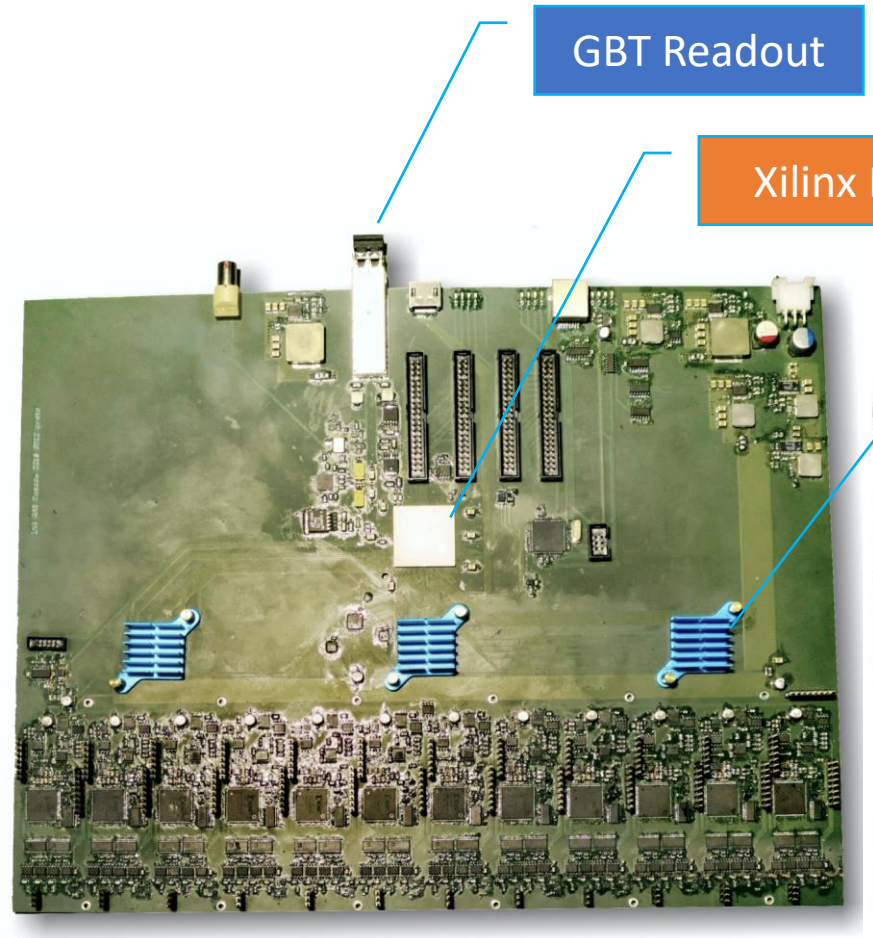




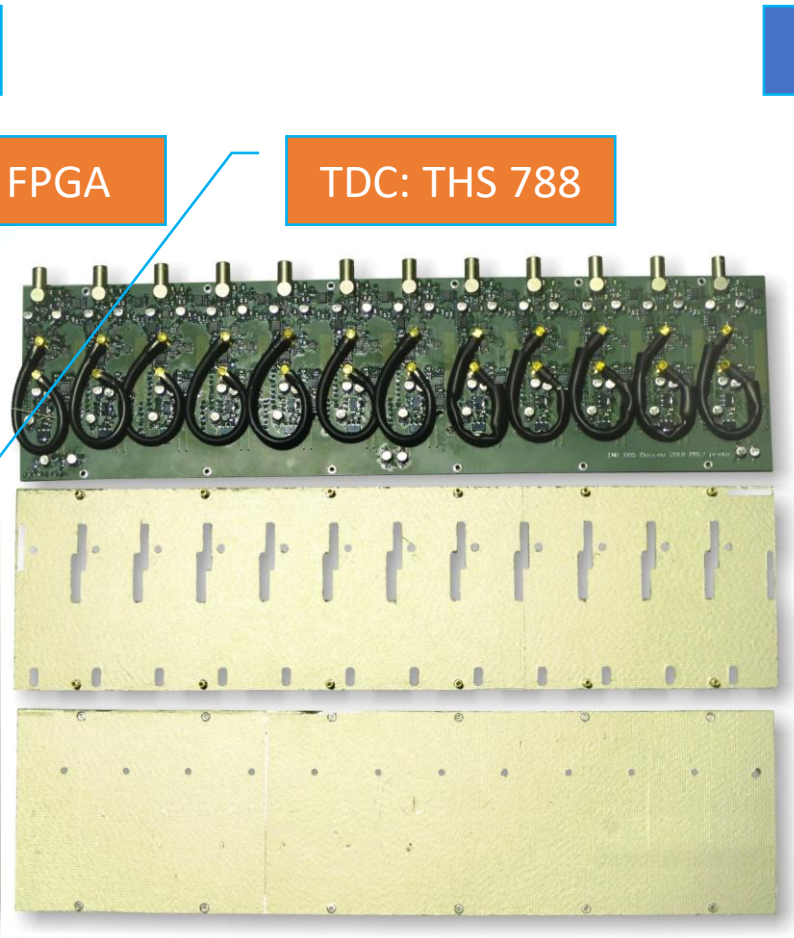


Comparison of threshold triggering (left) and constant fraction triggering
(en.wikipedia.org/wiki/Constant_fraction_discriminator)

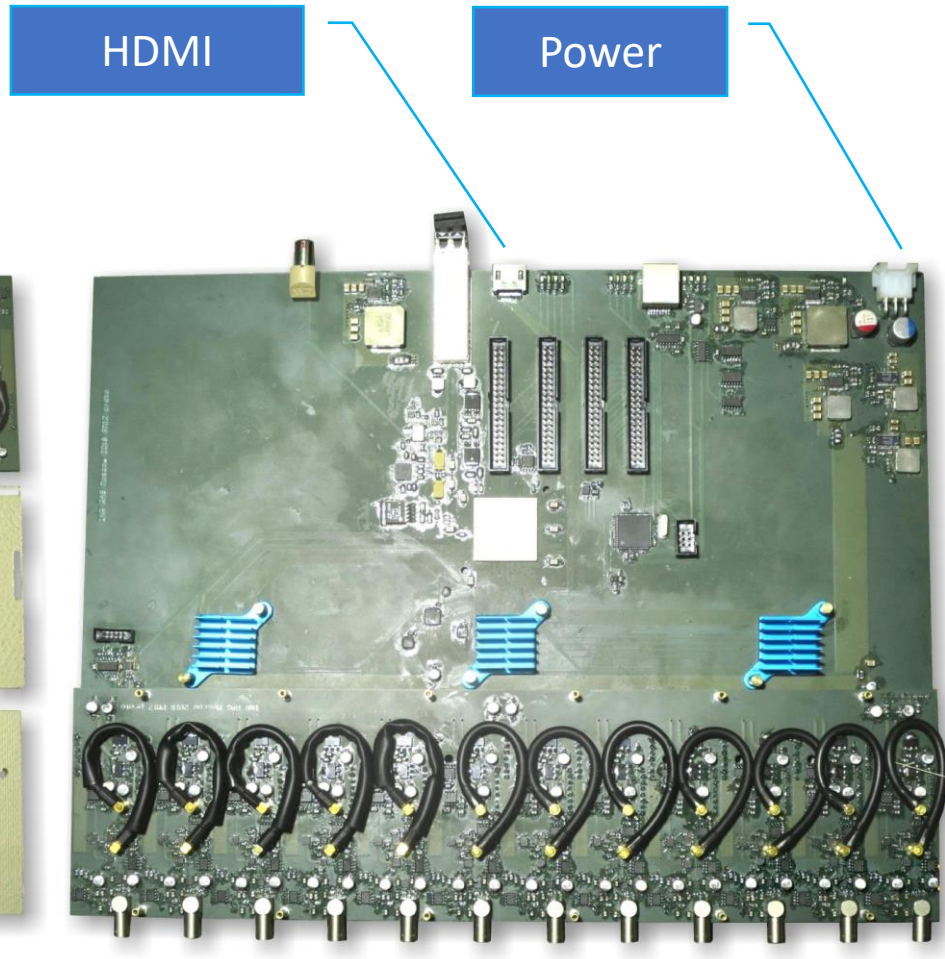
PM board assembly



Main PM board

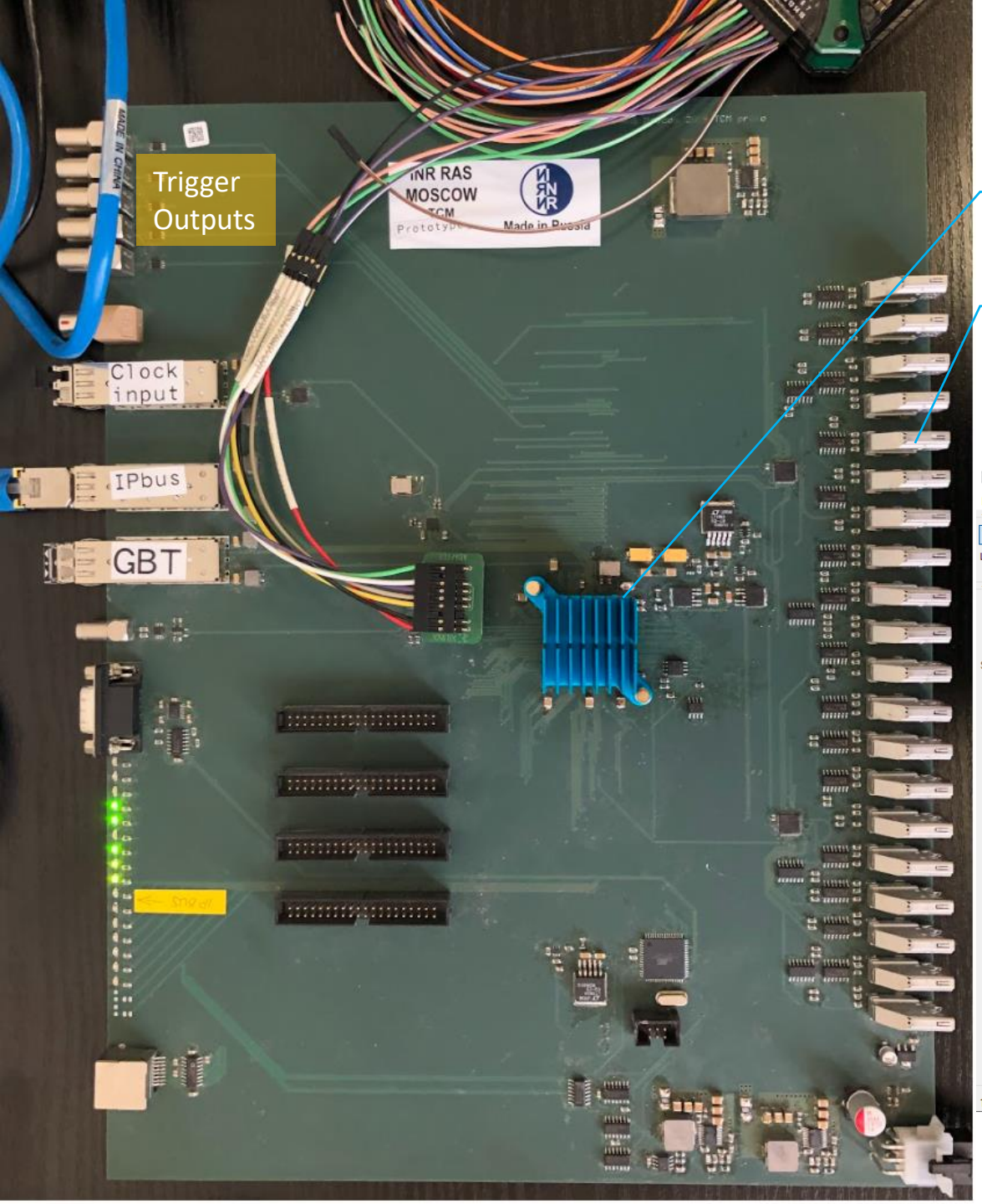


Mezzanine & shields



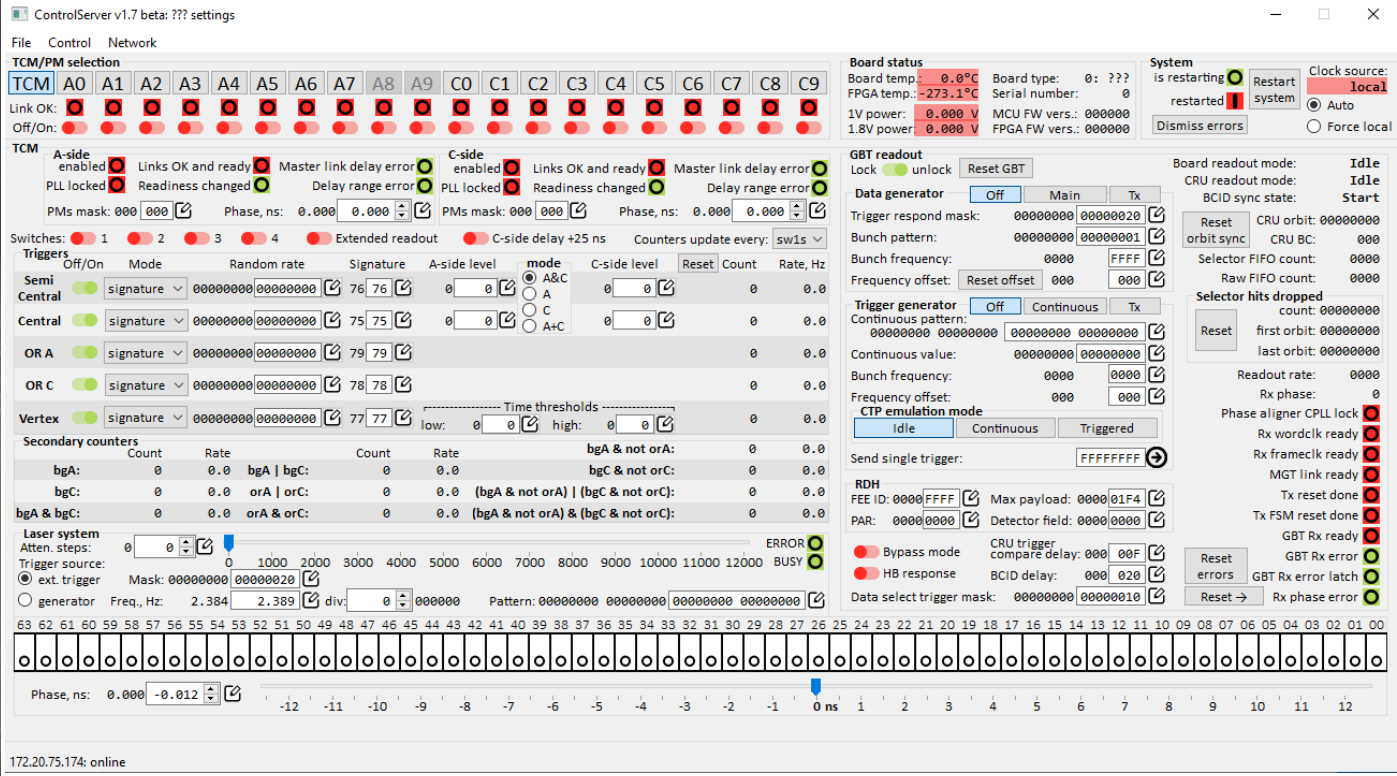
Assembled PM board

TCM board@AGH



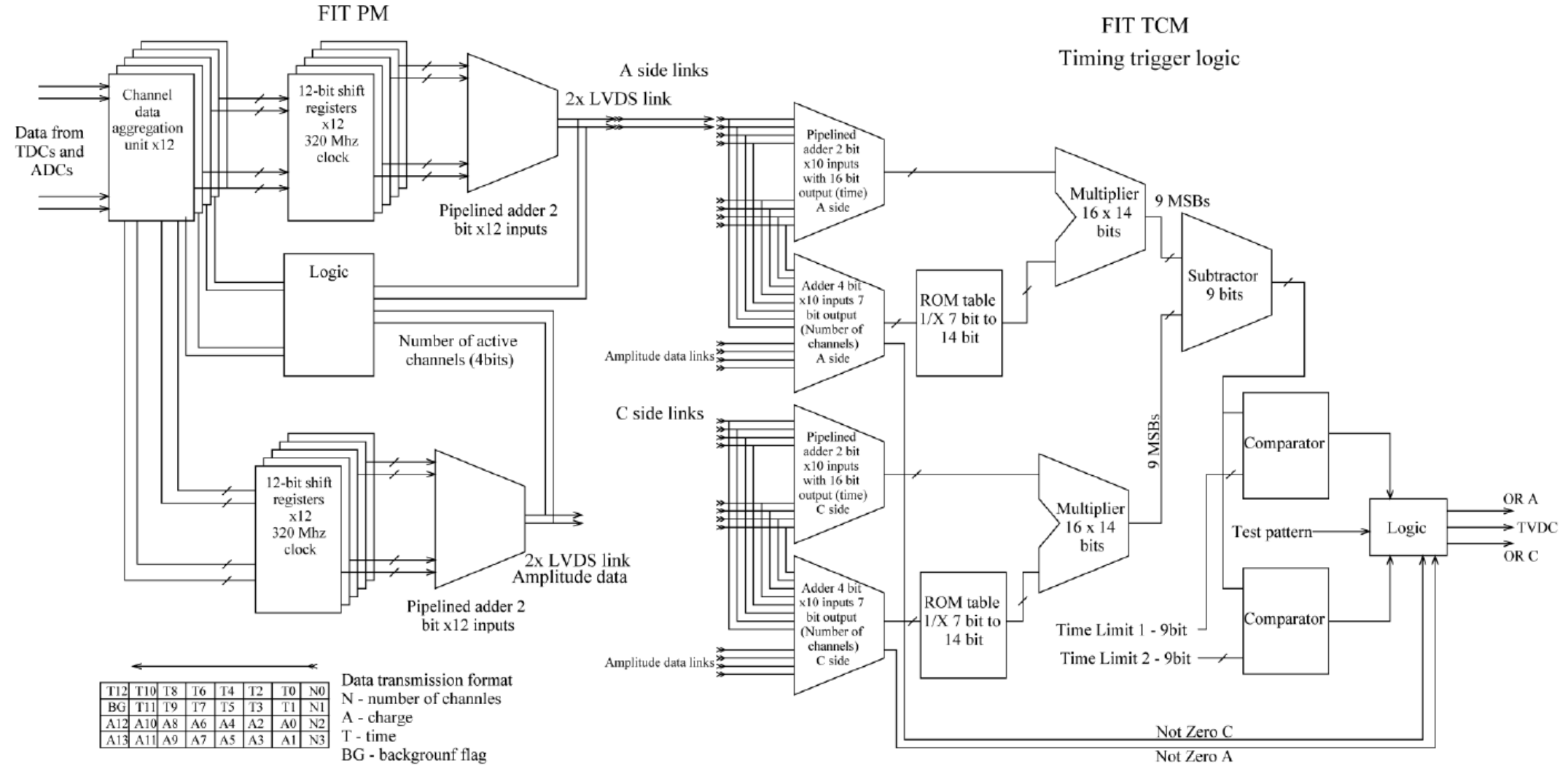
Xilinx FPGA

20×HDMI



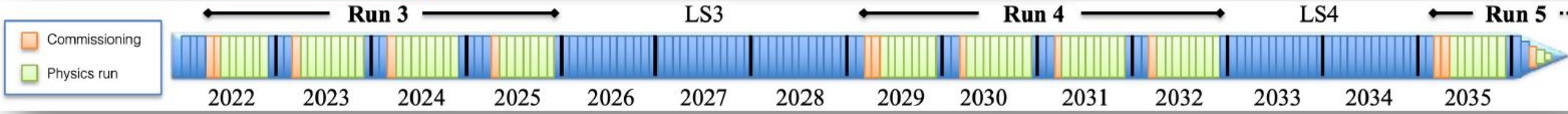
Control server

Trigger Logic and Timing



CERN management plan for FIT future

RU@CERN



Adaptation of mezzanine boards for FV0 and FDD. Noise removal and better FEE dynamics

Mid-term

Further adaptation of mezzanine boards for FV0 and FDD before nominal luminosity

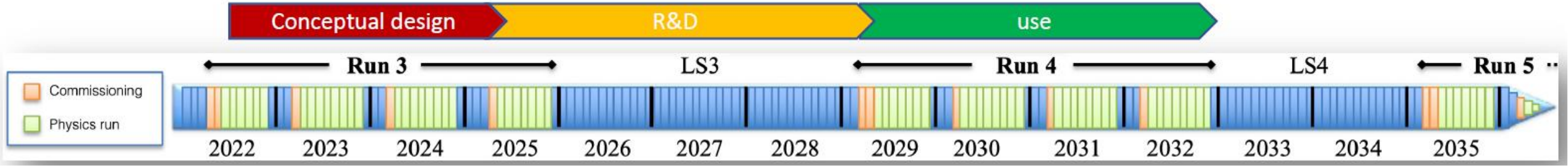
Long-term (end of Run 4)

New electronics.
- Higher resolution
- Better flexibility

- Increase involvment of AGH
- Introduction of WUT as a new member of ALICE
- Efforts financed by grant from Polish Ministry and CERN

Long term plan for FIT electronics

- Based on the experience gained from FT0, FV0 and FDD electronics, to develop new electronics (≤ 20 ps time resolution)
- New electronics developed, tested, installed, and comissioned during long shutdown LS3 (2026-2028)
- New FEE ready for Run4 (2Q'2029)



Short and medium term plan for FIT electronics

- Short and medium term plan regards current electronic hardware.
- Problem! Full documentation is not avaliable. Non-conventional approch is necessary,
- but the INR group still works very actively
- Support for current hardware (PMs and TCMs)
  - It is necessary despite INR future in FIT!
  - Prepare ourselfs for production and calibration of replacement PM and TCM boards (in case INR group is not avaliable)
- Design of the new mezzanine analog front end from scratch to mitigate known problems of FV0 and FDD

Near future ALICE-PL activities (July/August)

Ongoing efforts to aquire funds for short and long term activities

- possible CERN money involvement
- grant proposal for Polish Ministry

Setup of AGH & WUT colaboration

- discussions/meetings – in progress
- grant proposal should be prepared soon
- preliminary: AGH -> firmware
- our ambition: AGH -> hardware/firmware

Things for duscussion

New people/groups necessary in ALICE-AGH

- experience in high frequency analog/digital design (Institute of Electronics)
- experience in HEP electronics (Faculty of Physics and Applied Science AGH)

Identify experts and areas where we can/want to help

- short, mid, and long term tasks

Introduction of new AGH experts to ALICE and FIT management

- Power-point presentation of the new AGH experts has to be prepared (next week)
- Participation in planned grant-related discussions

Quick jump of the new people into the project

- visit of the new people in FIT laboratory in CERN (August/September)