



Studies of The Opto-Electronic Chain for The LHCb RICH Upgrade

Igor Ślazyk

University of Ferrara

&

Institute of Nuclear Physics Polish Academy of Sciences

Introduction

During my joint Ph.D. studies between the University of Ferrara (Italy) and the Institute of Nuclear Physics Polish Academy of Sciences (Poland), I had an opportunity to work in the LHCb experiment at CERN.

My research activities focused on the LHCb Ring-Imaging Cherenkov (RICH) detectors upgrade. The ultimate goal of my Ph.D. was to test the newly developed photodetection units, called the **Elementary Cells** (ECs).

For these reasons, I took part in the following activities:

- Development of the experimental test setup for quality control of the ECs,
- Software development of the automated software for the ECs quality assurance,
- Hardware testing and assembly of the ECs,
- Quality control measurements of the ECs,
- Preparation of protocols and manuals,
- Preparation of scripts and offline data analysis,

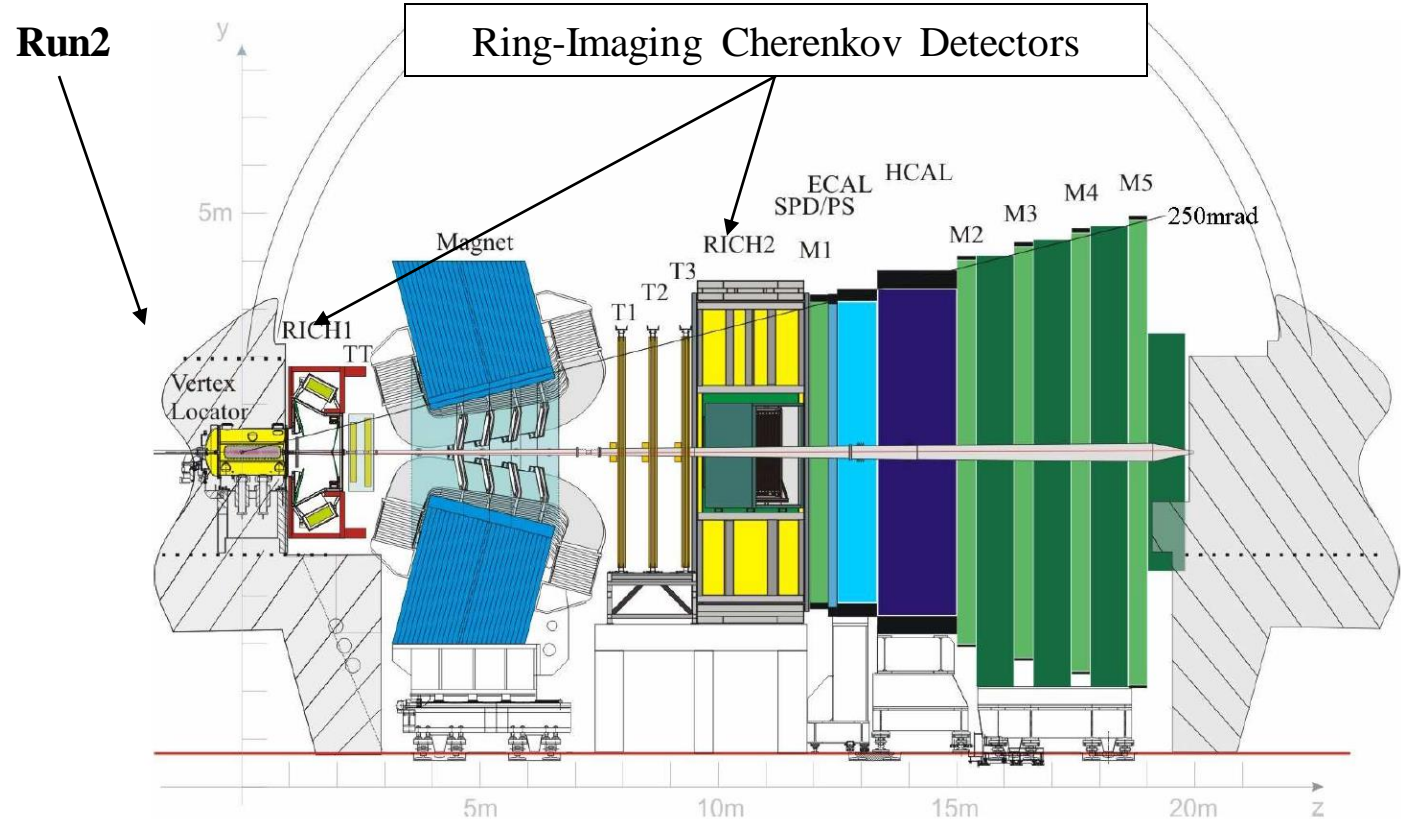
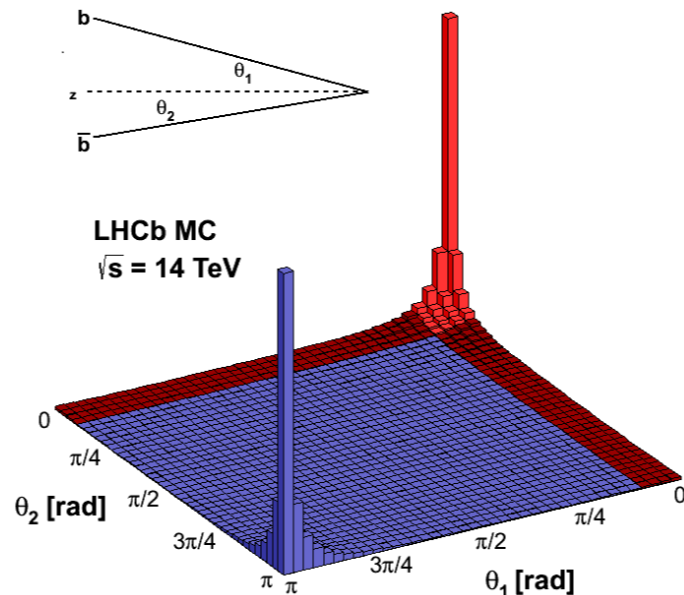
In this presentation, I would like to show you the overview of the **Elementary Cell Quality Assurance** (ECQA) performed in Ferrara.

The LHCb Experiment at CERN

Overview

LHCb deals with heavy flavour physics

- General-purpose detector in forward region
- Goals:
 - Measure CP-violation in b-sector
 - Search for the rare decays
 - Exploit forward production of b-pairs with low angle
- Such studies can help to understand the matter-antimatter asymmetry in our Universe.



LHCb RICH detectors: RICH1 and RICH2

Particle Identification (PID)

- Separate charged hadrons to select decays of interest: kaons, pions and protons

The LHCb Experiment at CERN Upgrade (1)

Reasons for the upgrade:

- More data to further challenge theoretical predictions
- Expose of detectors to radiation damage over years
- **Bottleneck of Level-0 hardware trigger (1.1 MHz)**
- **Change in parameters → new geometry**

LHCb Upgrade:

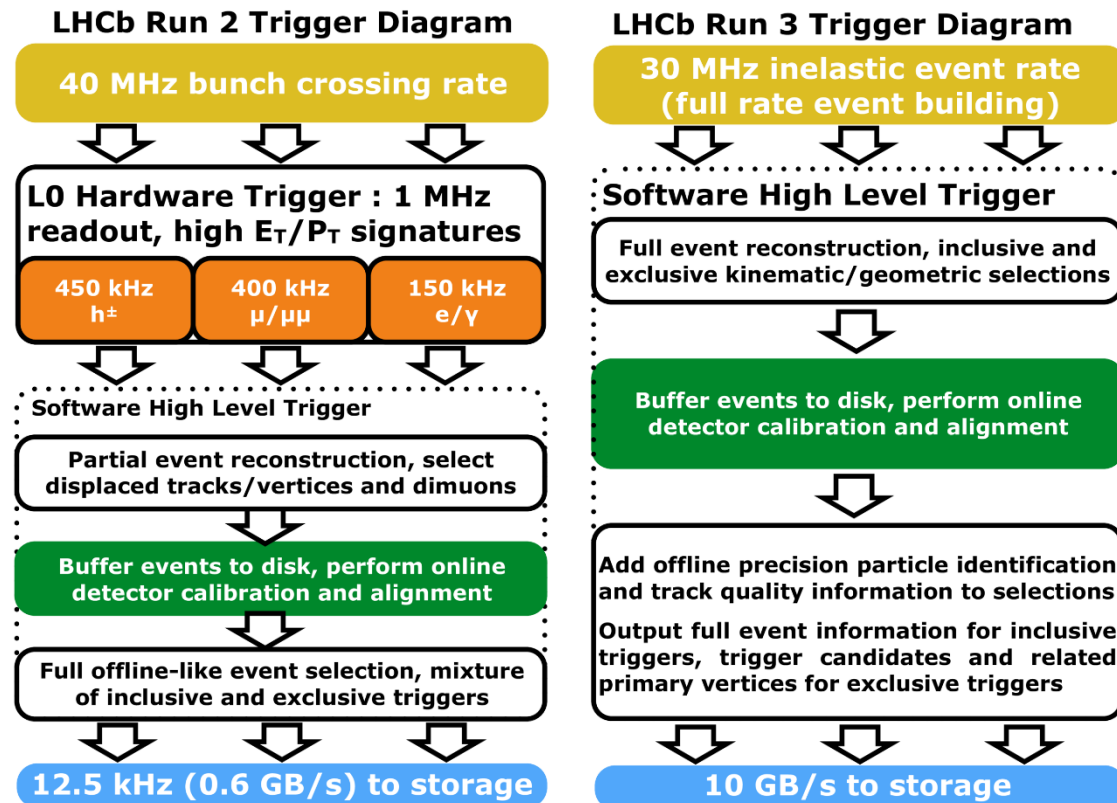
$$\mathcal{L} = 4 * 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$$

$$\mathcal{L} = 2 * 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$$

$$f = 1 \text{ MHz}$$

$$f = 40 \text{ MHz}$$

- Replacement of L0 hardware trigger with software trigger
- Adjustments in geometry, change in read-out electronics



We are here

Large Hadron Collider (LHC)

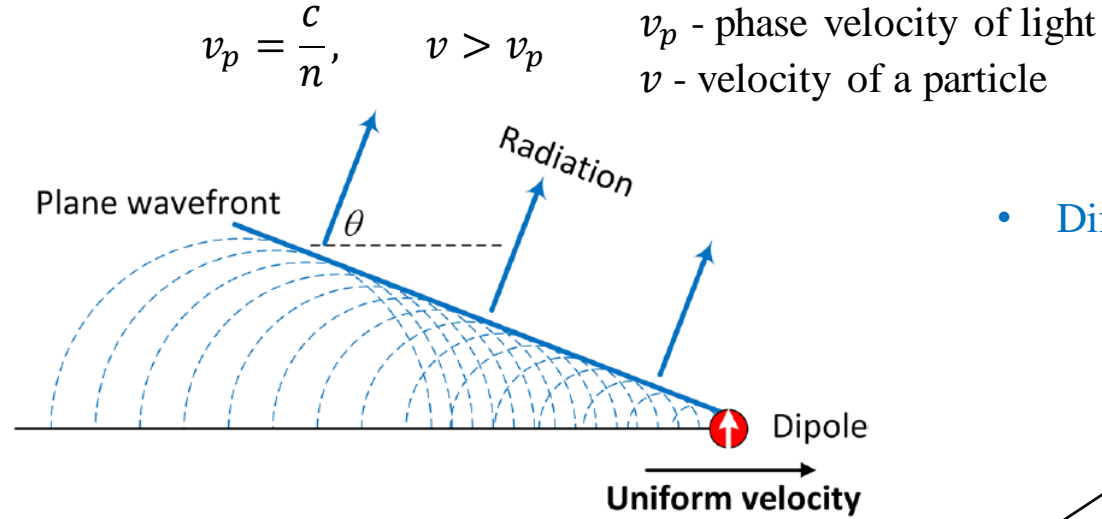
HL-LHC



The LHCb Experiment at CERN

Cherenkov Radiation

- Charged particles faster than light in a dielectric medium



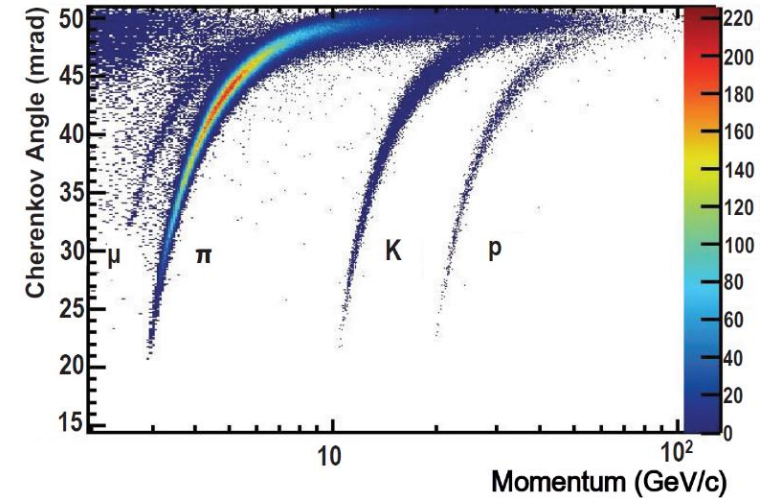
- Different characteristics of particles → precise identification

- Energy emitted as photons: **Cherenkov photons**
- Cherenkov angle:

$$\cos \theta = \frac{v_p}{v} = \frac{1}{\beta n}, \quad \beta = \frac{v}{c}$$

- Mass of a particle:

$$\cos \theta = \frac{1}{n} \sqrt{\left(\frac{m}{p}\right)^2 + 1} \quad \rightarrow \quad m = p \sqrt{n^2 \cos^2 \theta - 1}$$



- Most particles in RICH detectors: protons, pions and kaons.

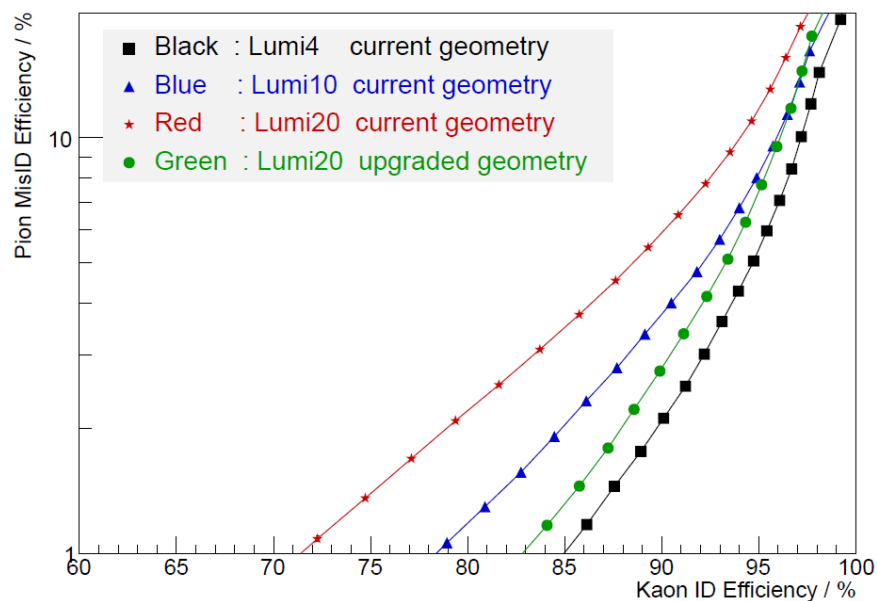
The LHCb Experiment at CERN

Importance of the PID

Channel	Branching fraction
$B_s^0 \rightarrow D_s^\mp K^\pm$	$(0.23 \pm 0.02) \times 10^{-3}$
$B_s^0 \rightarrow D_s^- \pi^+$	$(3.04 \pm 0.23) \times 10^{-3}$
$B^0 \rightarrow D^- \pi^+$	$(2.57 \pm 0.13) \times 10^{-3}$
$\bar{\Lambda}_b^0 \rightarrow \bar{\Lambda}_c^- \pi^+$	$(4.9 \pm 0.4) \times 10^{-3}$

signal

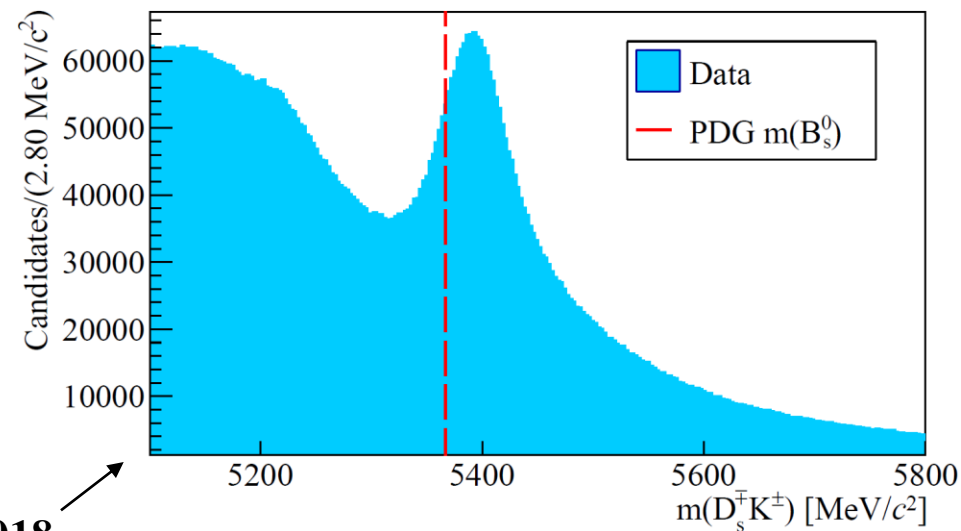
background
contamination



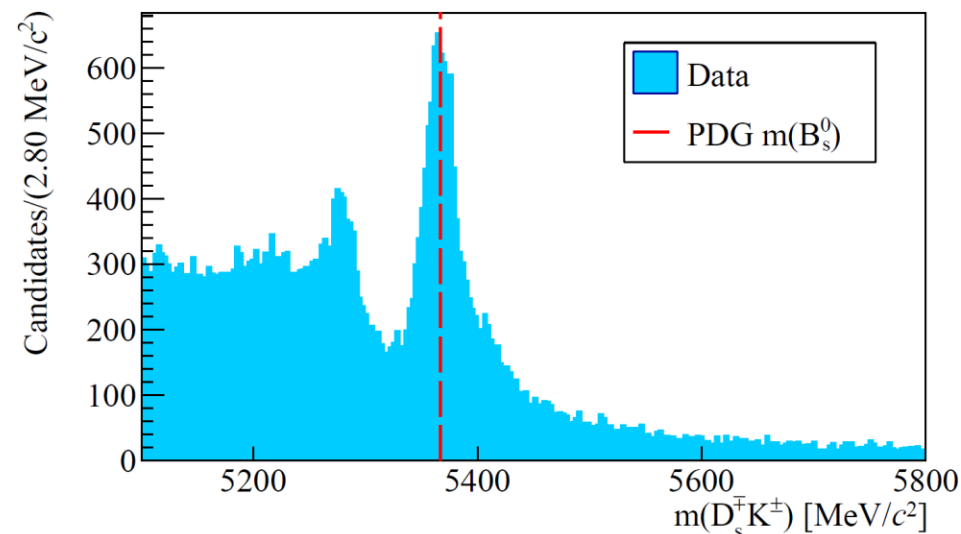
Lumi4 $3.9 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$

Lumi10 $10 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$

Lumi20 $20 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$



Data from 2018



The LHCb RICH Detectors

Pre-upgraded

RICH1

- Acceptance: 25 – 300 mrad
- Momentum range: $\sim 1 - 60$ GeV/c
- Refractive index: 1.0014 (C_4F_{10})

RICH2

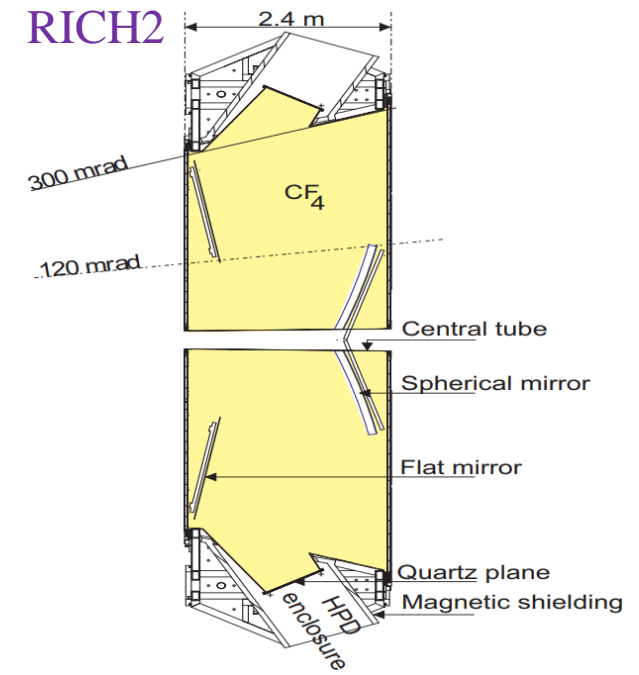
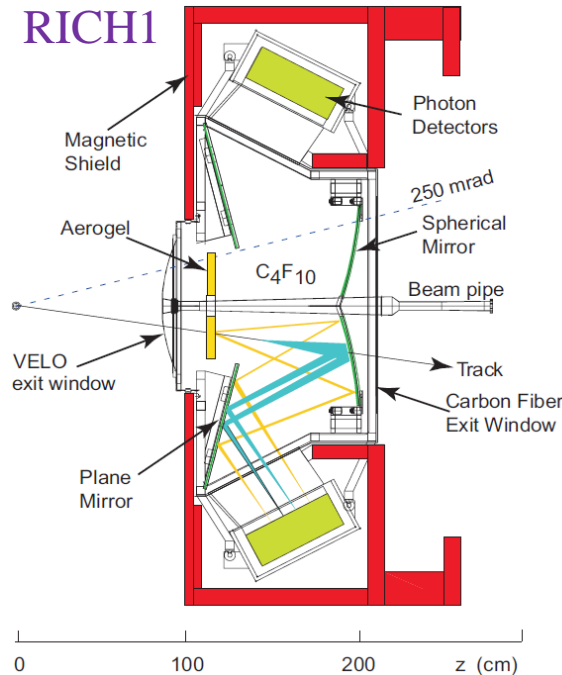
- Acceptance: 15 – 120 mrad
- Momentum range: $\sim 15 - 100$ GeV/c
- Refractive index: 1.0005 (CF_4)

Optical system:

- **Hybrid Photon Detectors (HPDs)**
- Spherical mirrors and flat mirrors

HPDs:

- Vacuum photodetectors
- Accelerated photoelectrons dissipated in silicon
- Each HPD has 1024 pixels (32×32 matrix), each pixel's size: $500 \mu m \times 500 \mu m$
- **Front-End (FE) electronics at 1 MHz bonded to pixel sensor**



The LHCb RICH Detectors Upgrade Overview

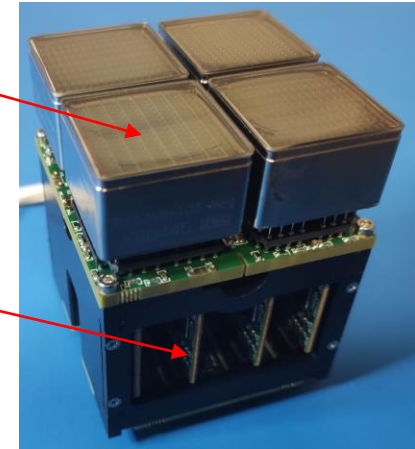
Change of the photon detectors:

- HPDs replaced by **Multi-Anode Photomultiplier Tubes (MaPMTs)**

Change in FE readout electronics:

- **CLARO** amplifier / discriminator ASIC
- FPGA-based digital boards
- GigaBit Transceiver (GBT) chip

New photon detection unit → **Elementary Cells (EC)**

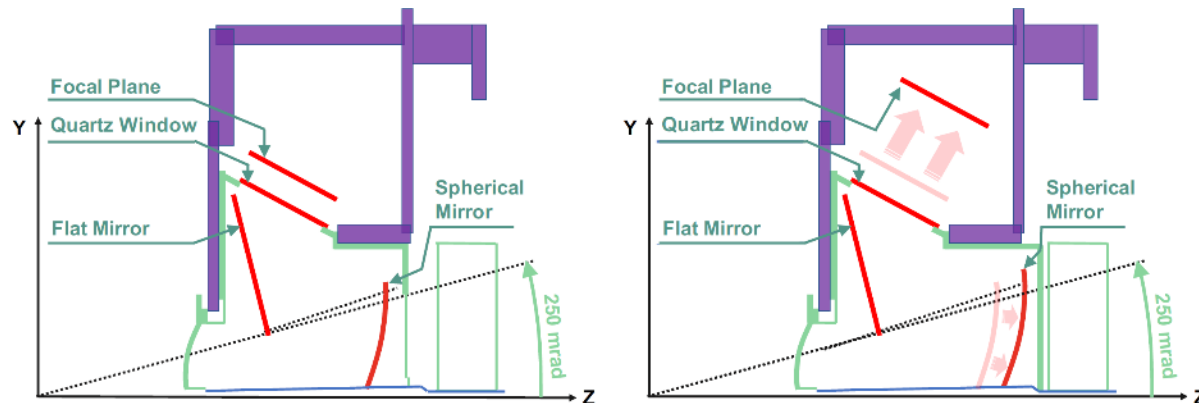


6.6 cm

RICH1 modifications:

- **Redesign of mechanics**
 - new support
 - new cooling
- **Optimization in optics**
 - spherical mirrors focal length increase
 - spherical and plane mirrors repositioned

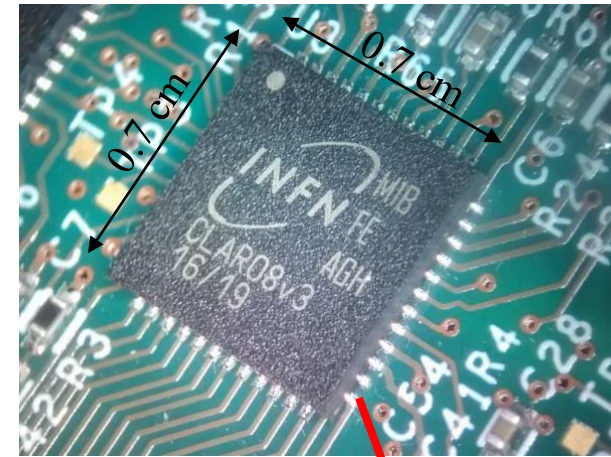
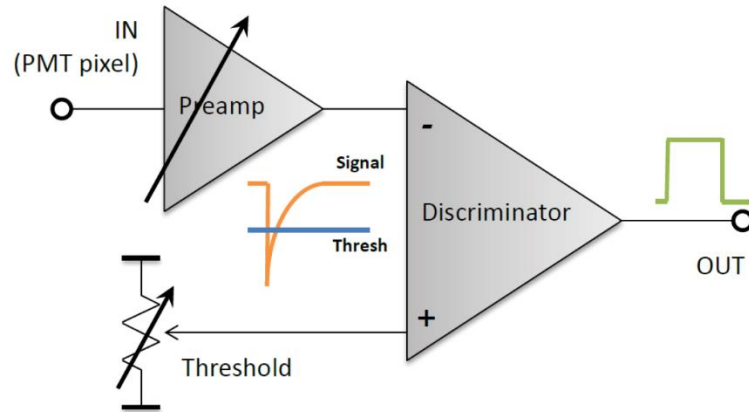
↓
peak occupancy < 30 %



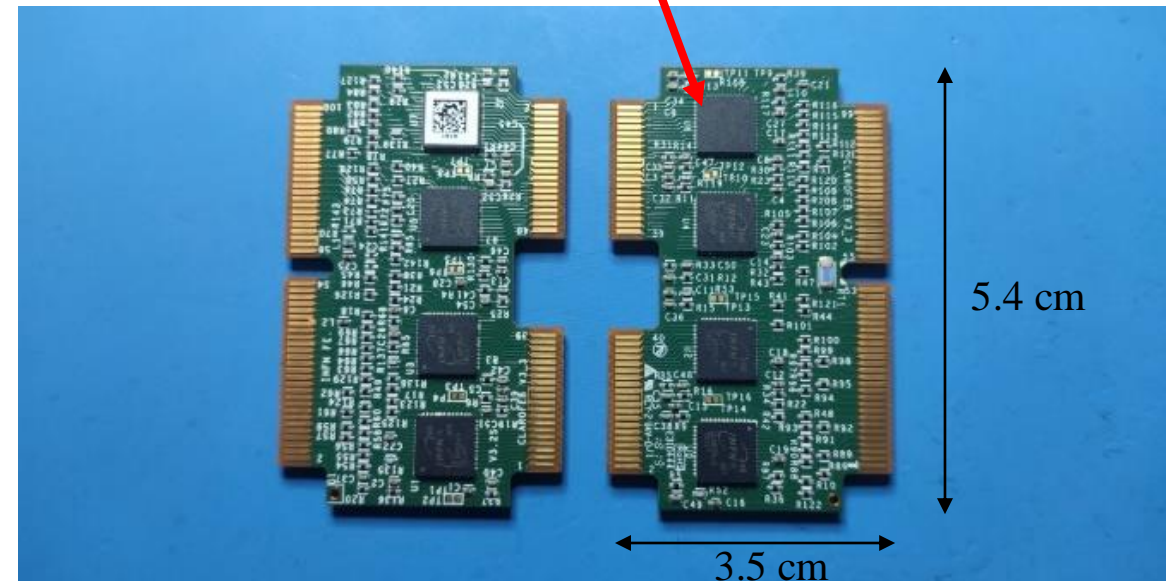
The LHCb RICH Detectors Upgrade CLARO

The CLARO chip:

- Designed by: AGH Kraków, INFN Ferrara, INFN Milano Bicocca
- **8 channel** amplifier / discriminator ASIC (0.35 μm CMOS, AMS)



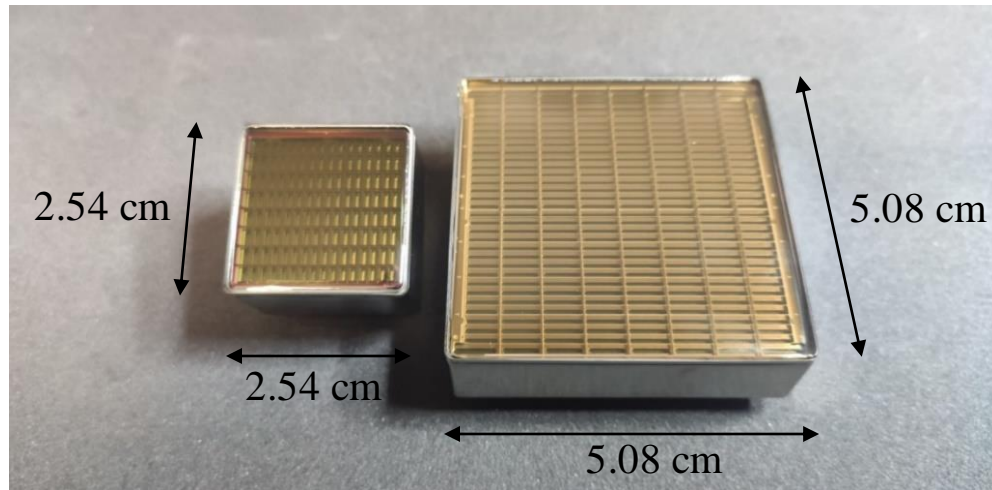
- Single photon counting with MaPMTs
- 40 MHz operation (recovery time < 25 ns)
- Low power consumption (< 1 mW per channel)
- Radiation-tolerant
- Mounted on Front-End Board (FEB)
- 8 chips per 1 FEB \rightarrow 64 channels



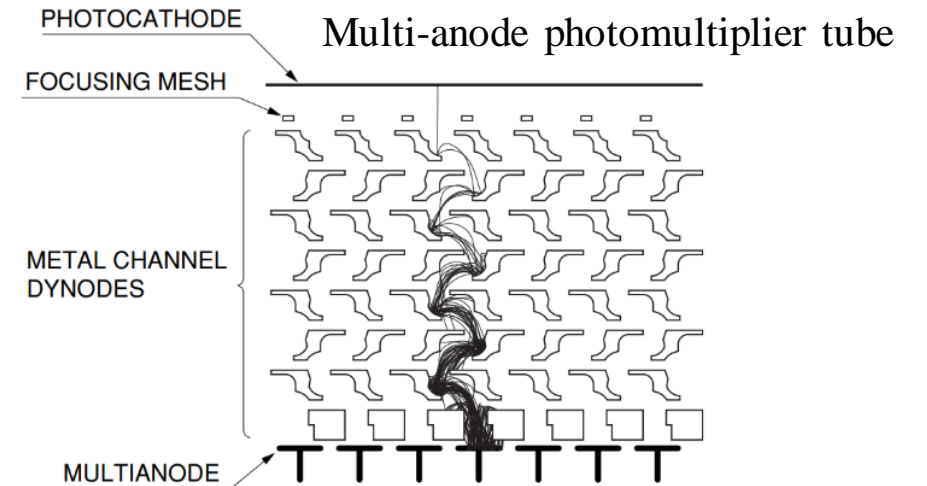
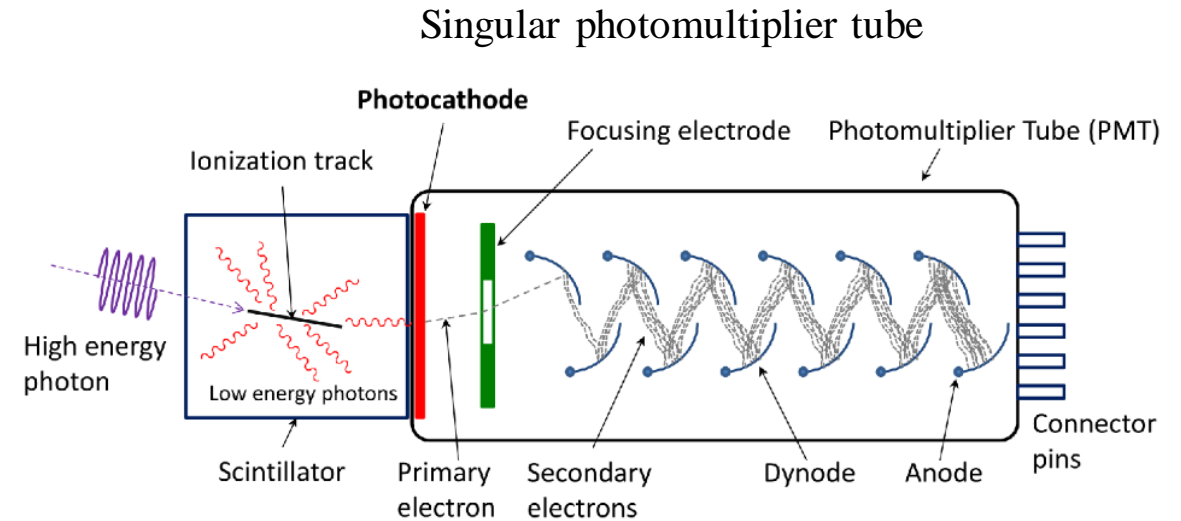
The LHCb RICH Detectors Upgrade Multi-Anode Photomultiplier Tube

MaPMT:

- Two types of MaPMTs designed by Hamamatsu Photonics:
 - **R13742 MaPMT** from R11265 series (1") – **R-type**
 - **R13743 MaPMT** from R12699 series (2") – **H-type**

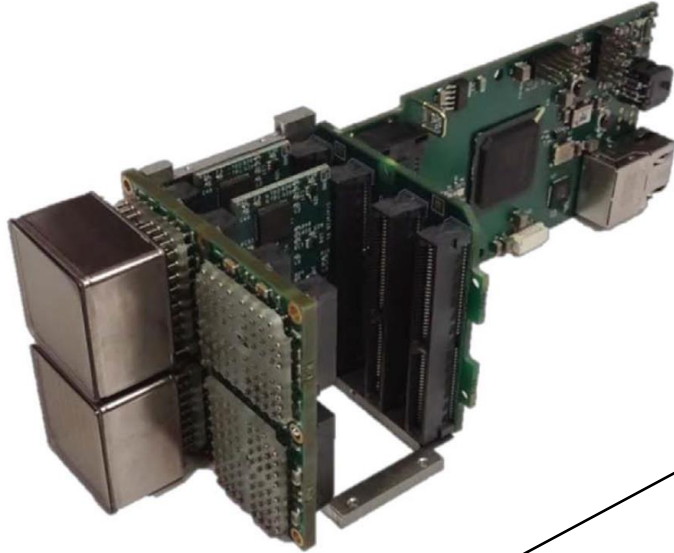


- **Single photon counting**
- Large active area → 2.9 mm × 2.9 mm (R-type), 6 mm × 6 mm (H-type)
- **8 × 8 anode matrix** → 64 silicon pixels
- Low dark count rate
- 12 stages of dynodes
- Typical gain of $10^6 e^-$ at 1000 V

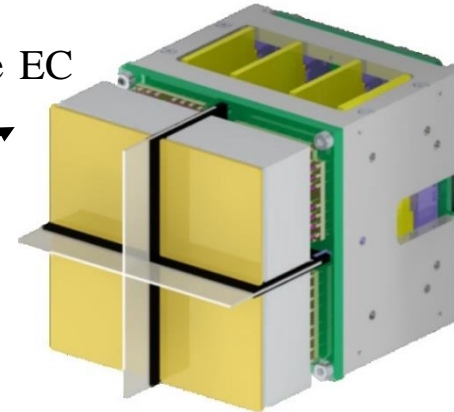


The LHCb RICH Detectors Upgrade Elementary Cell

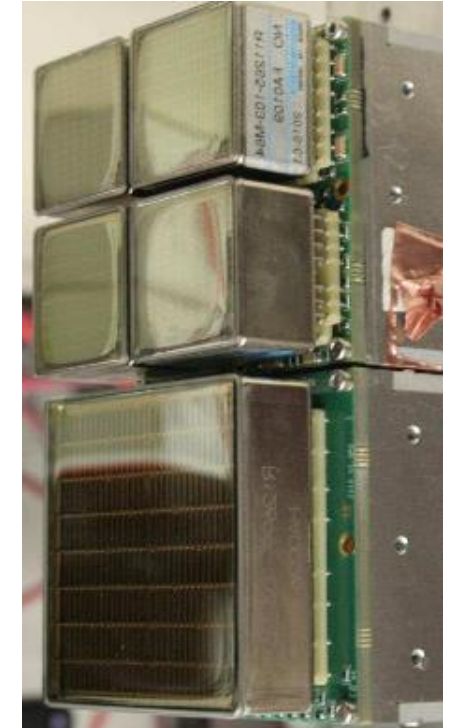
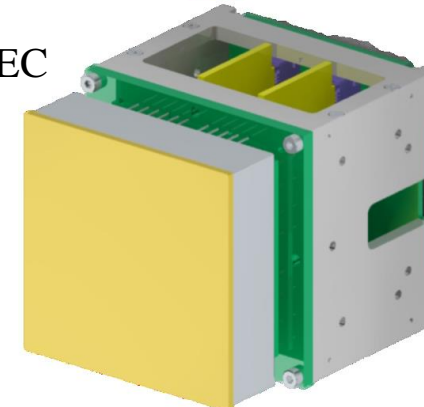
EC is the basic building unit of the RICH detection system.



R-type EC



H-type EC

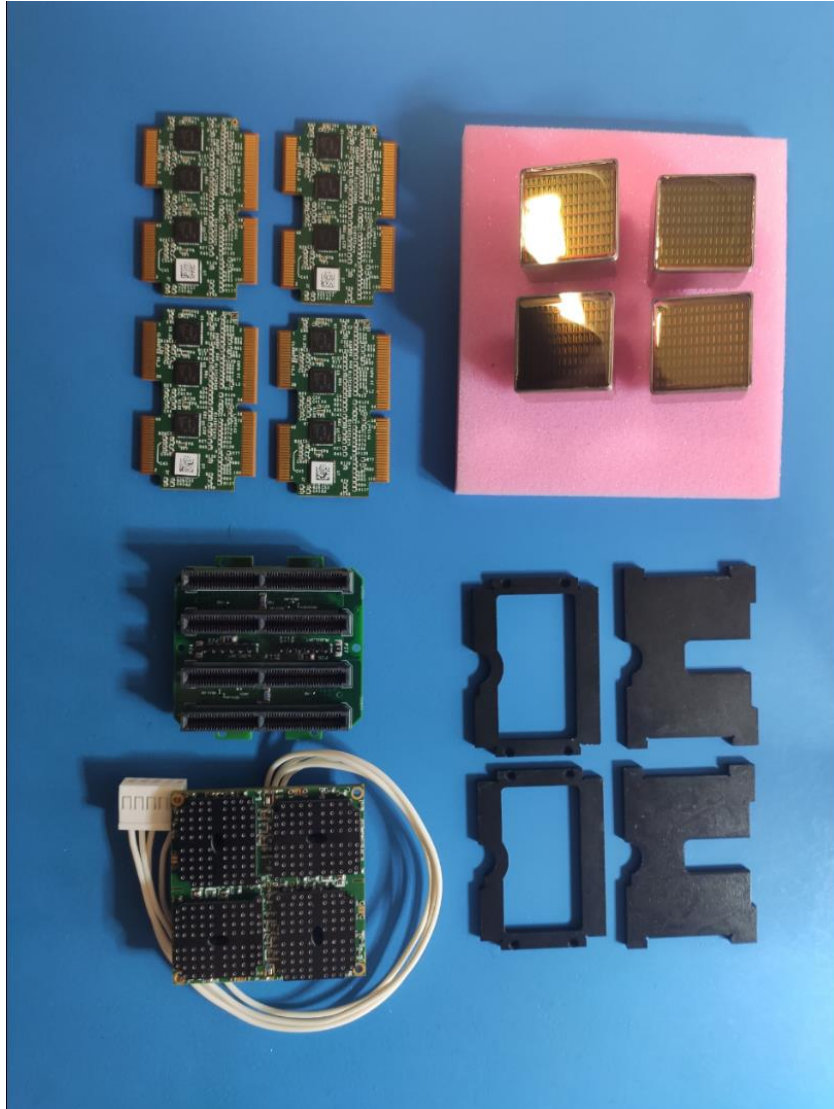


Components:

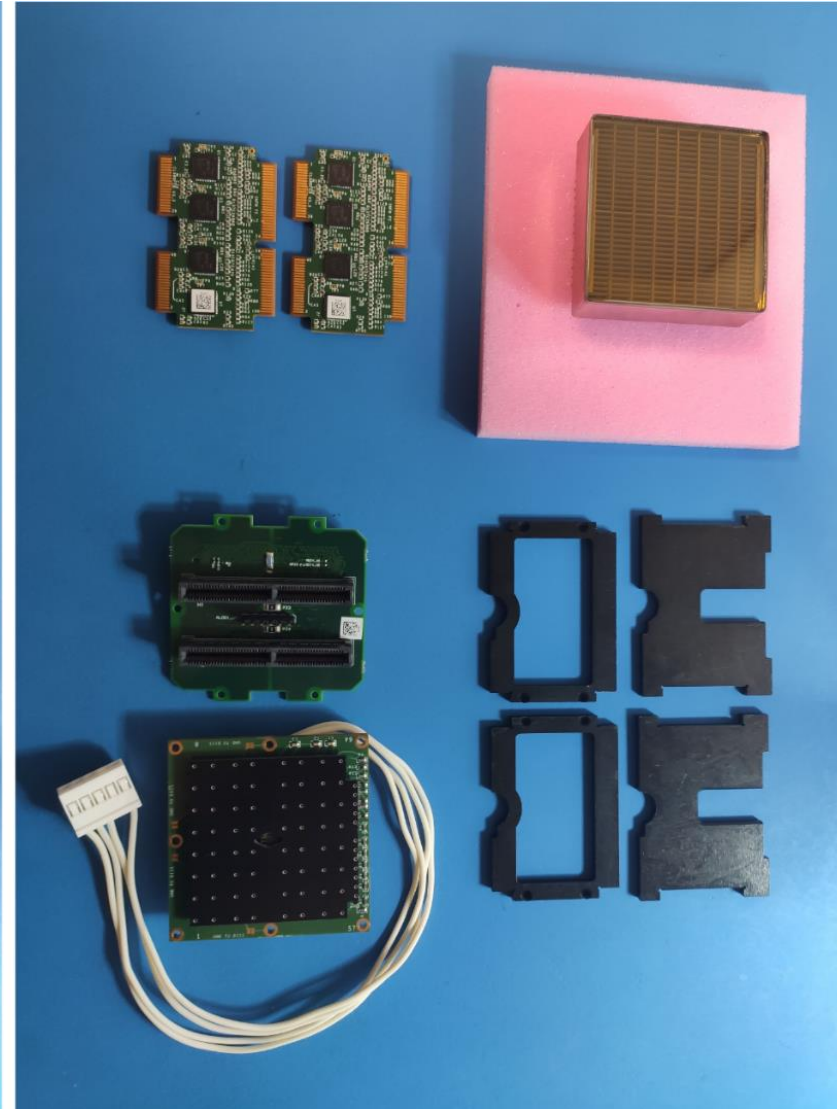
- 2x2 Hamamatsu R13742 (1")
- 1x1 Hamamatsu R13743 (2")
- Baseboard (Bb) interfacing MaPMTs with Front-End Boards (FEBs)
- 8 CLARO chips mounted on FEB
- Backboard (Bkb) interfacing FEBs with digital boards (DBs)
- DBs with FPGA readout logic and ethernet external connectivity

The LHCb RICH Detectors Upgrade Components of Elementary Cell

R-type EC



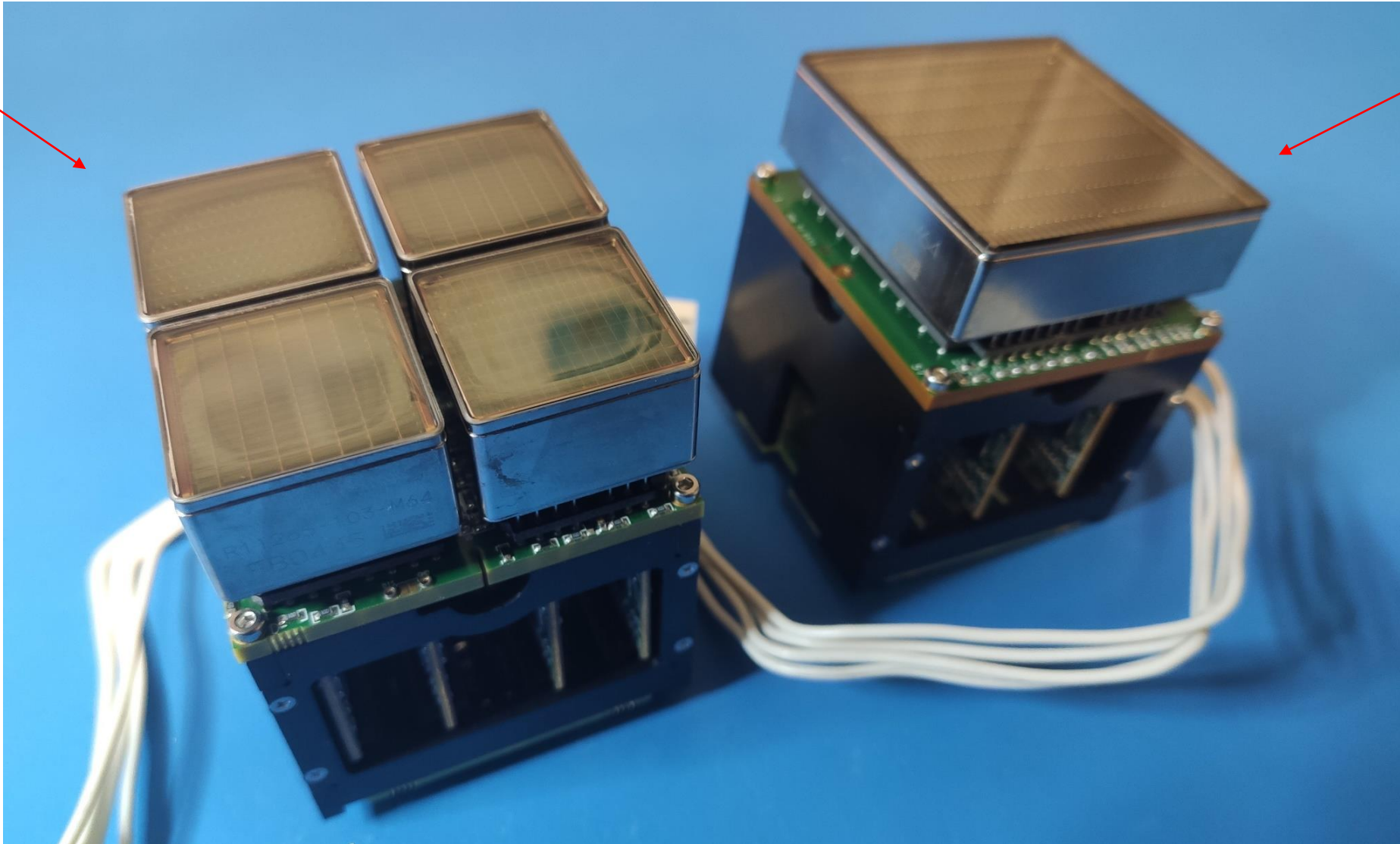
H-type EC



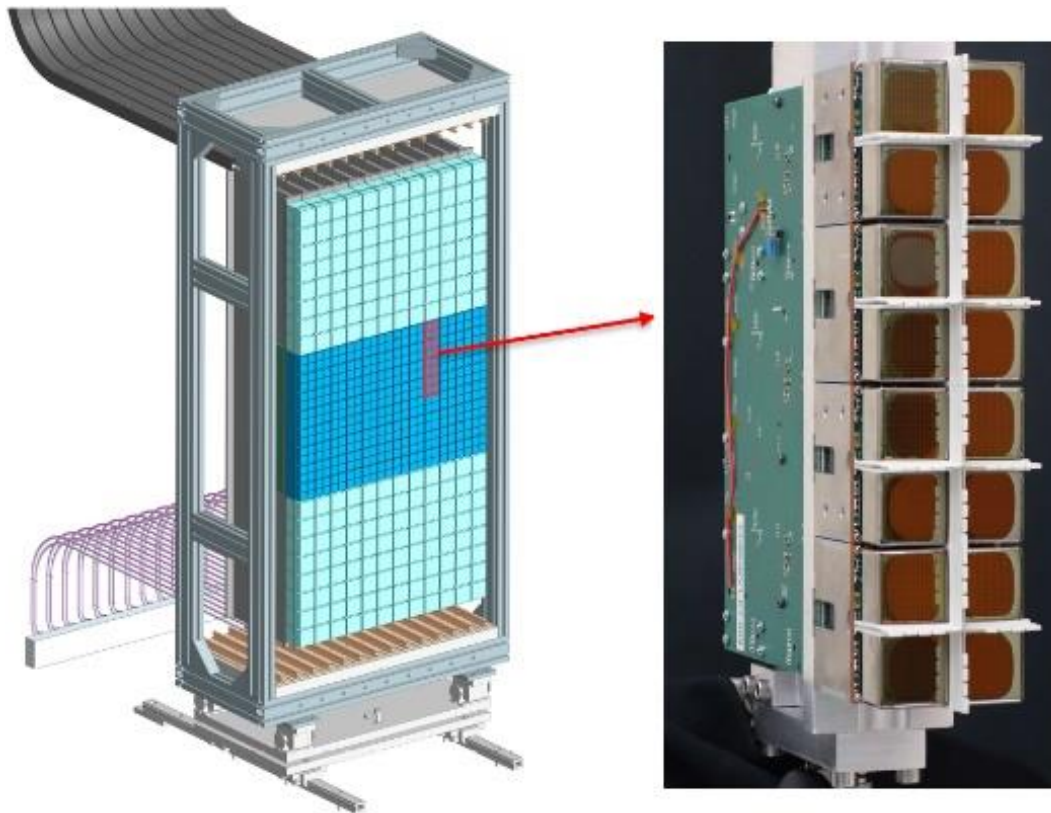
The LHCb RICH Detectors Upgrade Assembled Elementary Cells

R-type EC

H-type EC



The LHCb RICH Detectors Upgrade Photodetector Columns and Planes



	ECs		MaPMTs	
	R-Type	H-Type	R-Type	H-Type
RICH1	480	-	1920	-
RICH2	192	384	768	384
RICH1 + RICH2	672	384	2688	384
	1056		3072	



Elementary Cell Quality Assurance Experimental Test Setup

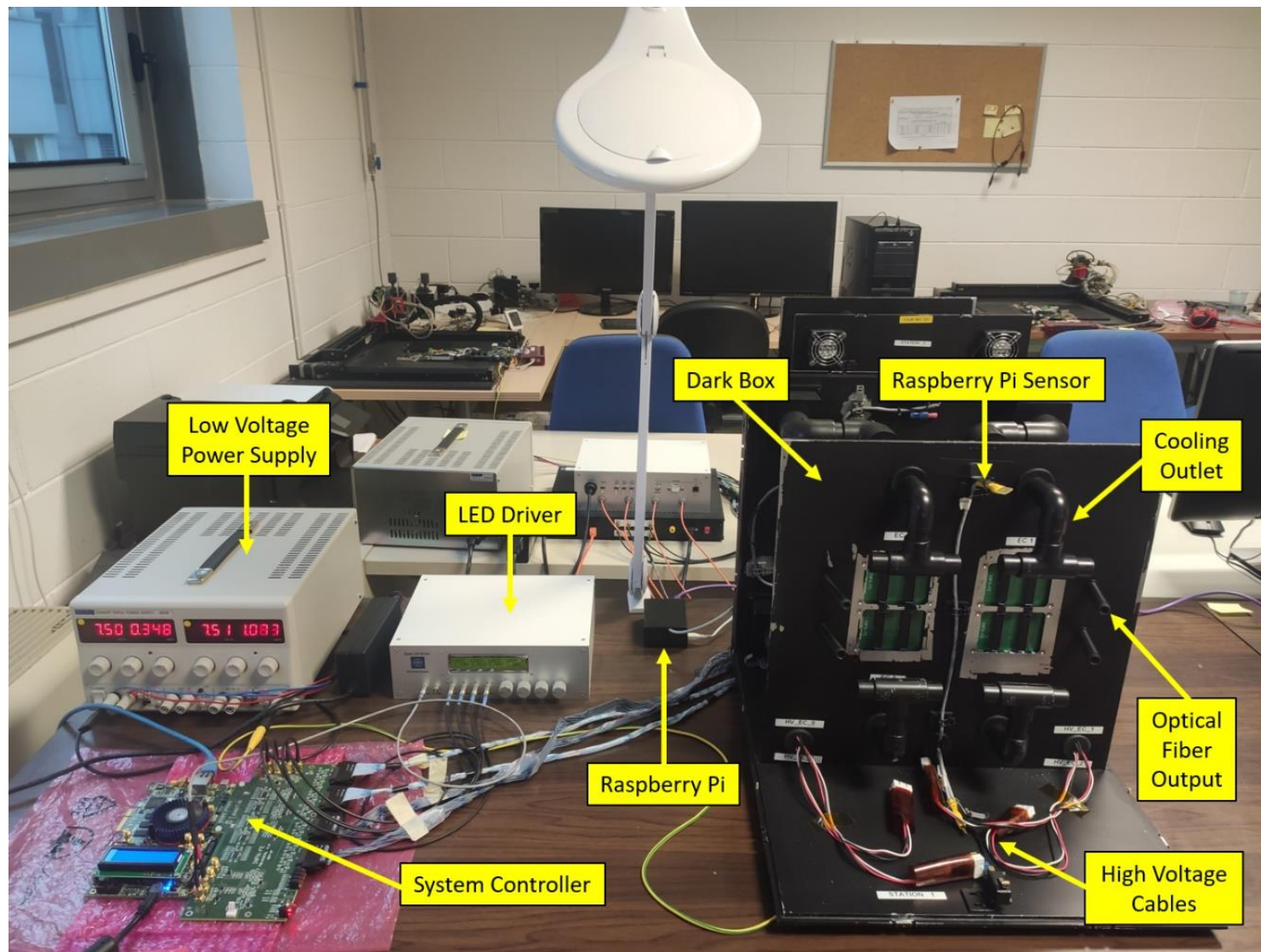
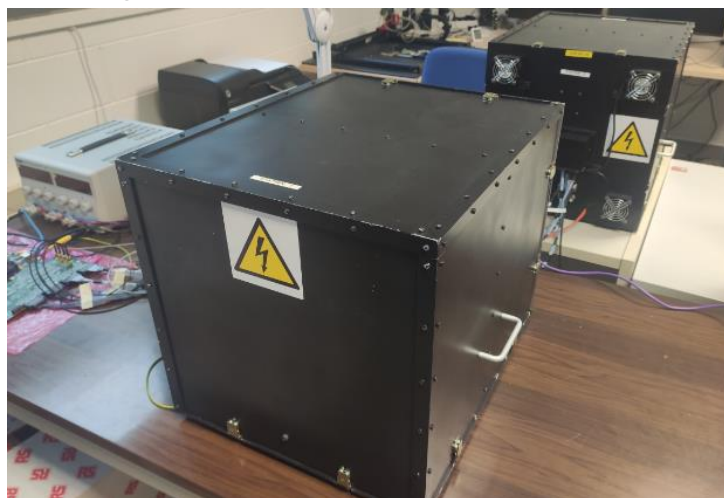
Authors: LHCb Ferrara Group
(myself included)

Test station:

- Dark Box
- LV power supply
- LED driver
- System controller
- Raspberry Pi
- HV ISEG crate

Facilities:

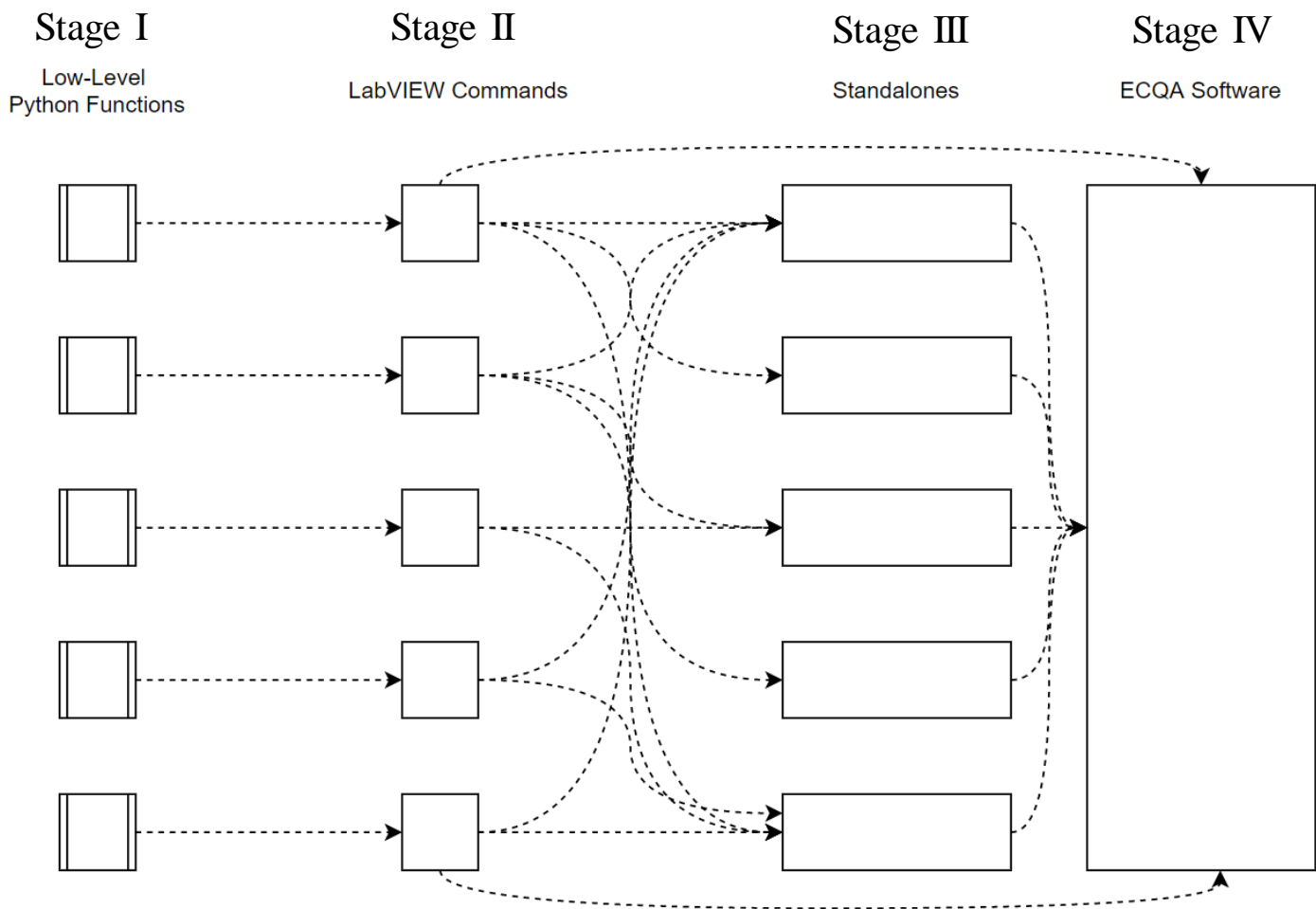
- Ferrara – Station 1 and 2
- Edinburgh – Station 3 and 4



Elementary Cell Quality Assurance Software – Overview

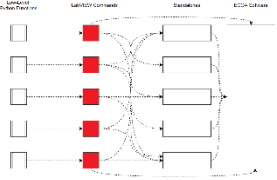
Authors: Igor Ślęzyk
Luca Minzoni
Edoardo Franzoso
Mirco Andreotti
Stefano Chiozzi

- Software development and debugging: nearly 2 years (2018-2019)
- Technologies: Python, C++ and LabVIEW



Elementary Cell Quality Assurance Software – Stage II (1)

Author: Igor Ślęzyk



- The lowest level: **python low-level functions**
- Upper level of hierarchy: **LabVIEW low-level sub-VIs (LabVIEW commands)** based on the **python low-level functions**
- **Communicates with hardware**

LabVIEW → python → system controller → FPGAs → hardware

Communication:

- Python-LabVIEW interface

Read:

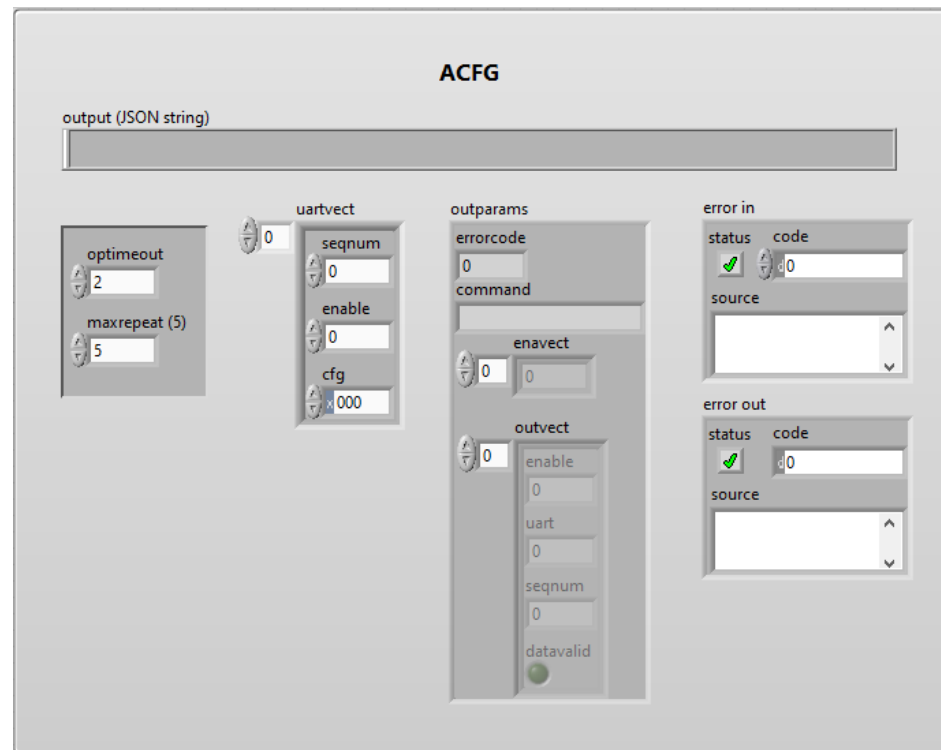
- Read hitcounts, counters, voltages, currents etc.

Write:

- Configuration of channels

Functionality:

- Selector of modules, power control, counter/hardware reset etc.

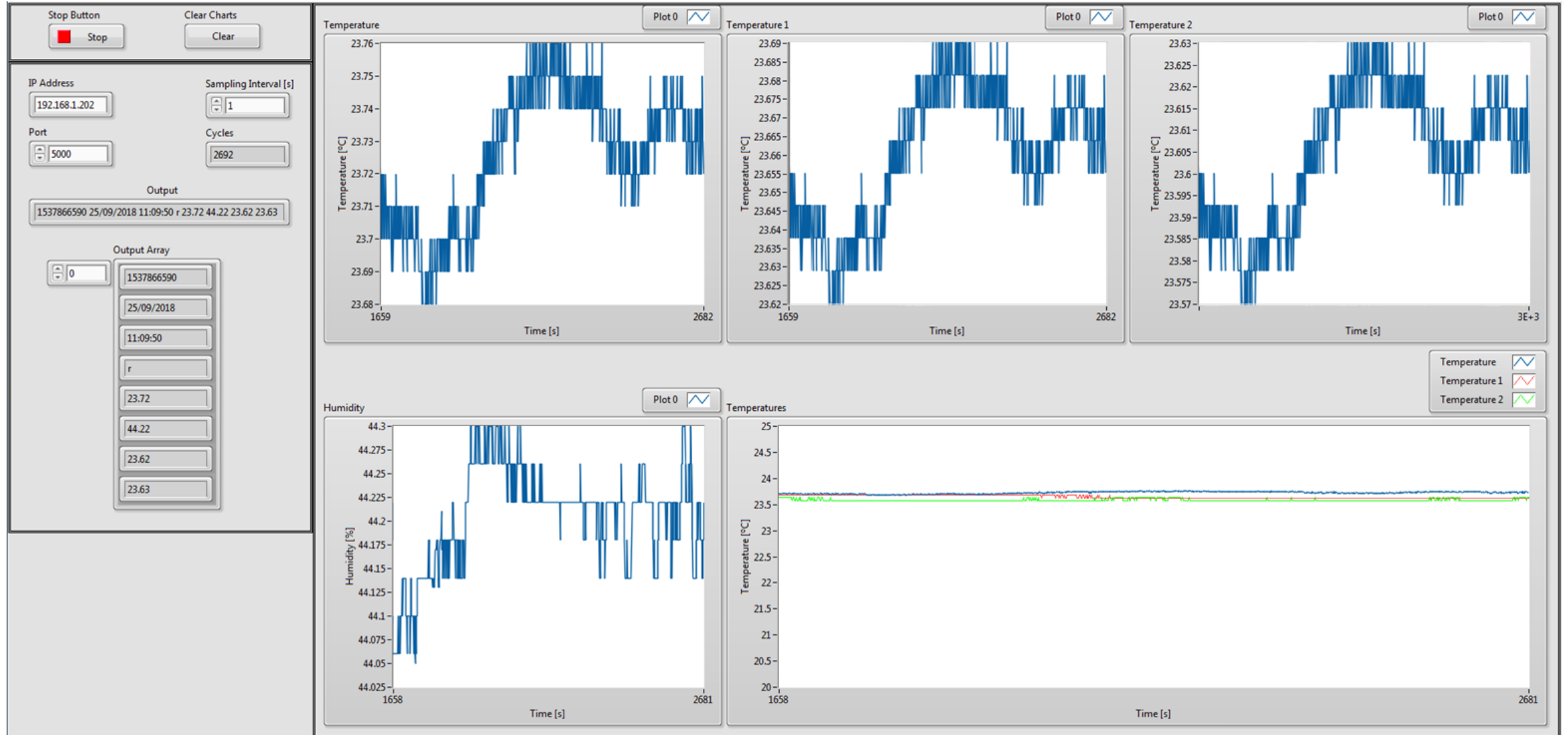
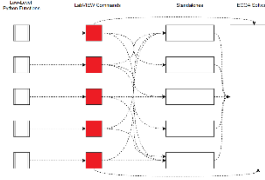


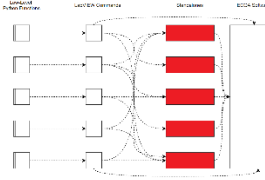
Temperature humidity reading software

Over 30 low-level python functions and corresponding LabVIEW commands

Elementary Cell Quality Assurance Software – Stage II (2)

Author: Igor Ślęzyk





Elementary Cell Quality Assurance Software – Stage III

Authors: Igor Ślęzyk
Luca Minzoni
Edoardo Franzoso

- Another upper level of hierarchy: **Standalones** based on the **LabVIEW low-level sub-VIs**
- Initial starting point of test measurements
- **Semi-automated DAQ software**
- **Implemented data analysis scripts**

Transition checker:

- Checking if transition is present for all the channels

Current measurements:

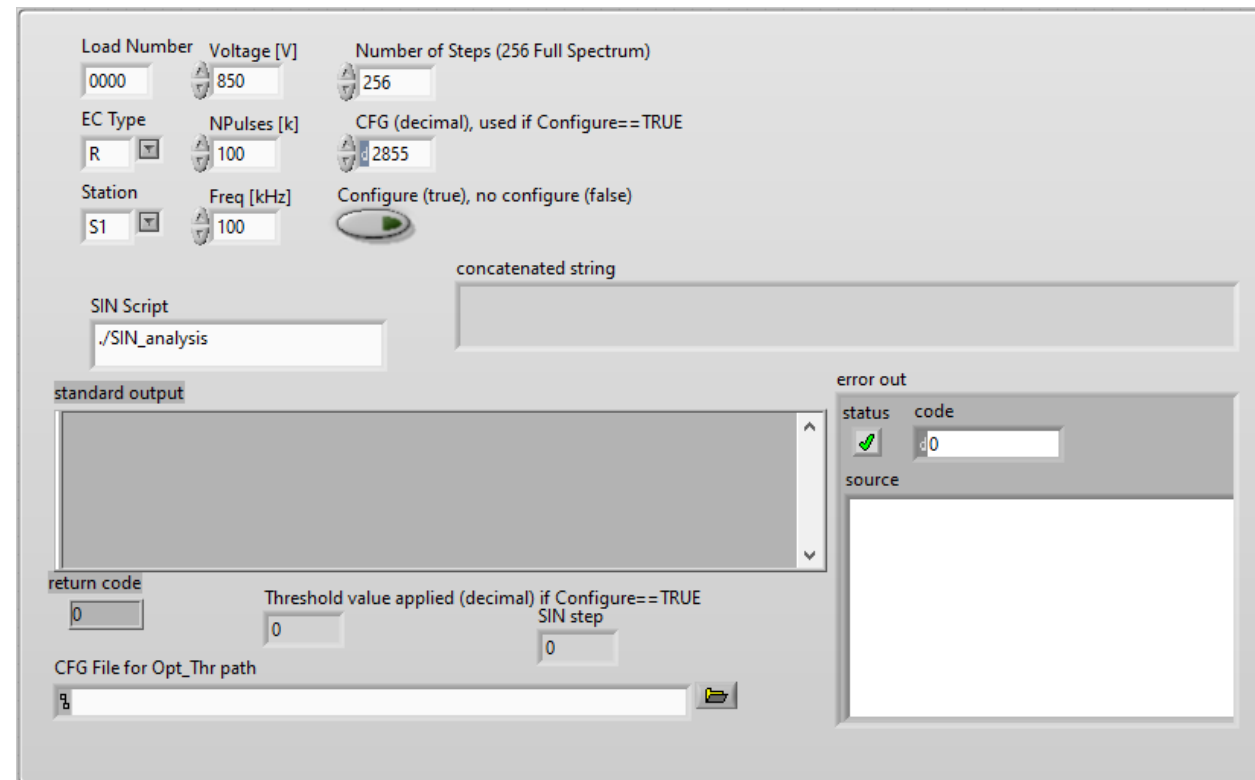
- Measurements of current and voltage

Quality assurance measurements:

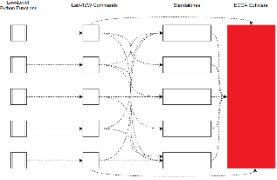
- Digital-to-Analog Converter Scan
- Threshold Scan
- Dark Count Rate
- Signal-Induced Noise

Configuration loader:

- Loads optimized configuration acquired from Threshold Scan



7 standalones

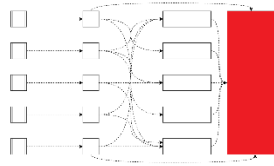


Elementary Cell Quality Assurance Software – Stage IV (1)

Author: Mirco Andreotti

- Final level of hierarchy: **ECQA software** based on the **Standalones** and **LabVIEW low-level sub-VIs**
- Maximum efficiency point of test measurements
- **Fully automated DAQ software**
- Test parameters initialization for all measurements at the very beginning
- Control and monitoring:
 - High voltage
 - Environmental (temperature and humidity)
- Offline data analysis scripts launched automatically after each test
- Manual operation only in case of critical errors and during the mounting procedure of the ECs and MaPMTs
- Approximate procedure time: 18 hours

Elementary Cell Quality Assurance Software – Stage IV (2)



MAIN CONTROL

DAQ STATE
Change setup
exec test **DISABLED**

STEP TEST STATE
SCAN PMTS **EXEC** auto/manual **MANUAL**

RPI SYSTEM

time	T	T1	T MAX	H MAX	T1 MAX	T2 MAX
04:23:35 PM 28/10/20	25.63	25.41	25.65	44.42	25.41	25.68
RUNNING	44.3	25.68	25.6	44.3	25.41	25.62
	H	T2	T MIN	H MIN	T1 MIN	T2 MIN

TEST ID CLUSTER

Test Station
TEST STATION 2
LOAD NUM
9999
EC TYPE
R TYPE

UserConfirmSTEP
CONFIRM STEP

S-Curve FAST NOT DONE

Check FEB curr CLARO comm NOT DONE

Check BaseBoard HV NOT DONE

SCAN PMTS RUNNING

S-Curve FAST NOT DONE

Check HV EC+PMT NOT DONE

S-Curve HV OFF NOT DONE

Keep HV ON Night NOT DONE

THR scan ERROR

Dark counts OPT THR NOT DONE

Dark counts COM THR NOT DONE

SIN SCAN OPT THR NOT DONE

TEST FINISHED NOT DONE

EC CODE RECOVERY NOT DONE

EC CODE RECOVERY NOT DONE

TEST LOG

```

2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 10 ; global_step 118/128 ; HV step 1/1 ; THR step 54/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 9 ; global_step 119/128 ; HV step 1/1 ; THR step 55/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 8 ; global_step 120/128 ; HV step 1/1 ; THR step 56/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 7 ; global_step 121/128 ; HV step 1/1 ; THR step 57/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 6 ; global_step 122/128 ; HV step 1/1 ; THR step 58/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 5 ; global_step 123/128 ; HV step 1/1 ; THR step 59/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 4 ; global_step 124/128 ; HV step 1/1 ; THR step 60/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 3 ; global_step 125/128 ; HV step 1/1 ; THR step 61/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 2 ; global_step 126/128 ; HV step 1/1 ; THR step 62/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 1 ; global_step 127/128 ; HV step 1/1 ; THR step 63/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:22 - THR SCAN: HV 1000 THR 0 ; global_step 128/128 ; HV step 1/1 ; THR step 64/64 ; offset bit 1 - ALREADY DONE
2020-10-28 16:17:33 - THR SCAN ANALYSIS DONE OK
2020-10-28 16:17:53 - OFFSET ANALYSIS DONE FAILED
2020-10-28 16:17:56 - THR SCAN ERROR
2020-10-28 16:19:41 - START SCAN PMTs OR CODES

2020-10-28 16:21:42 - INIT TEST
2020-10-28 16:21:43 - CONFIG TEST - LAST TEST NOT FINISHED - LOADING INFO...
2020-10-28 16:21:43 - CONFIG TEST DONE
2020-10-28 16:21:43 - CHECK STATUS LAST TEST
2020-10-28 16:21:48 - CHECK SETUP FILE
2020-10-28 16:21:48 - LOAD LAST SEUP
2020-10-28 16:21:48 - START SETUP CHECK
2020-10-28 16:21:53 - SETUP SAVED
2020-10-28 16:21:53 - INIT DEVICE
2020-10-28 16:21:53 - HV CONNECTION
2020-10-28 16:21:57 - LAST TEST RUNNING: HV PAR SET NOT DONE
2020-10-28 16:21:57 - LAST TEST RUNNING: HV POWER OFF NOT DONE
2020-10-28 16:21:57 - SYS CONTROLLER INIT
2020-10-28 16:22:02 - INIT DEVICE DONE OK
2020-10-28 16:22:46 - START SCAN PMTs OR CODES
    
```

SCAN AND MOUNT PMTs FOLLOWING INDICATION

Dark counts OPT THR | S-Curve FAST | S-Curve at HV ON | HV NIGHT

EC CONFIG | Check FEB curr CLARO comm | Check Base-Board HV | Check HV EC+PMT | S-Curve at HV OFF | Dark counts COM THR | THR scan | SIN SCAN OPT THR | SIN SCAN COM THR

scurve start time: 00:00:00.000 PM MM/DD/YYYY
scurve stop time: 00:00:00.000 PM MM/DD/YYYY
SCURVE remaining time: 00:00:00
S CURVE DONE: 0 / 0
S CURVE TOTAL: 0

SCURVE STEP STATUS

THR 30A	DONE
THR 31A	DONE
THR B2A	DONE
THR B3A	DONE
THR B3E	DONE
THR 0	NOT DONE

RAW DATA FILES

- /home/lab0/DATALoad_0075_R_S1/SCURVE_ctg30A.txt
- /home/lab0/DATALoad_0075_R_S1/SCURVE_ctg31A.txt
- /home/lab0/DATALoad_0075_R_S1/SCURVE_ctg31E.txt
- /home/lab0/DATALoad_0075_R_S1/SCURVE_ctgB2A.txt

PARAM FILES

- /home/lab0/DATALoad_0075_R_S1/SCURVE_ctg30A_par.txt
- /home/lab0/DATALoad_0075_R_S1/SCURVE_ctg31A_par.txt
- /home/lab0/DATALoad_0075_R_S1/SCURVE_ctg31E_par.txt
- /home/lab0/DATALoad_0075_R_S1/SCURVE_ctgB2A_par.txt

PDF FILES

- /home/lab0/DATALoad_0075_R_S1/PDF/SCURVE_ctg30A_dist.pdf
- /home/lab0/DATALoad_0075_R_S1/PDF/SCURVE_ctg31A_dist.pdf
- /home/lab0/DATALoad_0075_R_S1/PDF/SCURVE_ctg31E_dist.pdf
- /home/lab0/DATALoad_0075_R_S1/PDF/SCURVE_ctgB2A_dist.pdf

LOG ERROR STRING

```

SCURVE HV OFF RUNNING: THR 30A ; step 1 / 6
2020-07-29 10:43:20 - START CONFIG 32BIT FEB CLK
2020-07-29 10:43:21 - 32BIT CLOCK CONF OK -
2020-07-29 10:43:21 - 32BIT FEB CONF OK -
2020-07-29 10:43:21 - END CONFIG 32BIT FEB CLK
2020-07-29 10:43:21 - START CONFIG 32BIT SYS CTL
2020-07-29 10:43:21 - 32BIT SYS CTL CONF OK -
2020-07-29 10:43:21 - END CONFIG 32BIT SYS CTL
2020-07-29 10:43:21 - START S-CURVE HV OFF
2020-07-29 10:54:29 - S-CURVE OK - FEB 0
2020-07-29 11:05:38 - S-CURVE OK - FEB 1
2020-07-29 11:05:42 - END S-CURVE HV OFF
SCURVE HV OFF RUNNING: THR 31A ; step 2 / 6
2020-07-29 11:05:42 - START CONFIG 32BIT FEB CLK
2020-07-29 11:05:42 - 32BIT CLOCK CONF OK -
2020-07-29 11:05:43 - 32BIT FEB CONF OK -
2020-07-29 11:05:43 - END CONFIG 32BIT FEB CLK
2020-07-29 11:05:43 - START CONFIG 32BIT SYS CTL
2020-07-29 11:05:43 - 32BIT SYS CTL CONF OK -
2020-07-29 11:05:43 - END CONFIG 32BIT SYS CTL
2020-07-29 11:05:43 - START S-CURVE HV OFF
2020-07-29 11:16:50 - S-CURVE OK - FEB 0
2020-07-29 11:28:00 - S-CURVE OK - FEB 1
2020-07-29 11:28:03 - END S-CURVE HV OFF
SCURVE HV OFF RUNNING: THR 31E ; step 3 / 6
2020-07-29 11:28:03 - START CONFIG 32BIT FEB CLK
2020-07-29 11:28:03 - 32BIT CLOCK CONF OK -
2020-07-29 11:28:04 - 32BIT FEB CONF OK -
2020-07-29 11:28:04 - END CONFIG 32BIT FEB CLK
2020-07-29 11:28:04 - START CONFIG 32BIT SYS CTL
2020-07-29 11:28:04 - 32BIT SYS CTL CONF OK -
2020-07-29 11:28:04 - END CONFIG 32BIT SYS CTL
2020-07-29 11:39:11 - S-CURVE OK - FEB 0
2020-07-29 11:50:20 - S-CURVE OK - FEB 1
2020-07-29 11:50:23 - END S-CURVE HV OFF
SCURVE HV OFF RUNNING: THR 31E ; step 4 / 6
    
```

SYSTEM CONTROLLER

Py DEAMON STARTED
NET OPEN OK
SYS CTL RUNNING

STEP_EXEC / STEP_TOTAL: 8 / 8
hit count time: 0 / 100000
SIN STEP / SIN-HV STEP TOT: 0 / 0
SIN-HV STEP / SIN-TW STEP TOT: 4 / 4
SIN-TW STEP / SIN-TW STEP TOT: 0 / 0

SYS CTL LOG

```

QUERY STATUS REG OK - FPGA 1 - READ 0x0000 - REF 0x0000
QUERY STATUS REG OK - FPGA 2 - READ 0x0000 - REF 0x0000
QUERY STATUS REG OK - FPGA 3 - READ 0x0000 - REF 0x0000
QUERY STATUS REG OK - FPGA 4 - READ 0x0000 - REF 0x0000
QUERY STATUS REG OK - FPGA 5 - READ 0x0000 - REF 0x0000
QUERY STATUS REG OK - FPGA 6 - READ 0x0000 - REF 0x0000
QUERY STATUS REG OK - FPGA 7 - READ 0x0000 - REF 0x0000
2020-10-28 16:22:00 - END QUERY AT INIT
2020-10-28 16:22:00 - START POWER ON
2020-10-28 16:22:00 - POWER ON EXE OK - PyErrorCode 0 ErrorCode 0 EmrString
2020-10-28 16:22:00 - POWER ON - STATUS REG OK - FPGA 0x0000- REG VALUE 0x2D00
2020-10-28 16:22:00 - POWER ON - CURRENT OK - FPGA 0 - CURRENT VALUE 0
2020-10-28 16:22:00 - POWER ON - STATUS REG OK - FPGA 0x0001- REG VALUE 0x2D00
2020-10-28 16:22:00 - POWER ON - CURRENT OK - FPGA 1 - CURRENT VALUE 0
2020-10-28 16:22:00 - POWER ON - STATUS REG OK - FPGA 0x0002- REG VALUE 0x2D00
2020-10-28 16:22:00 - POWER ON - CURRENT OK - FPGA 2 - CURRENT VALUE 0
2020-10-28 16:22:00 - POWER ON - STATUS REG OK - FPGA 0x0003- REG VALUE 0x2D00
2020-10-28 16:22:00 - POWER ON - CURRENT OK - FPGA 3 - CURRENT VALUE 0
2020-10-28 16:22:00 - POWER ON - STATUS REG OK - FPGA 0x0004- REG VALUE 0x2D00
2020-10-28 16:22:00 - POWER ON - CURRENT OK - FPGA 4 - CURRENT VALUE 0
2020-10-28 16:22:00 - POWER ON - STATUS REG OK - FPGA 0x0005- REG VALUE 0x2D00
2020-10-28 16:22:00 - POWER ON - CURRENT OK - FPGA 5 - CURRENT VALUE 0
2020-10-28 16:22:00 - POWER ON - STATUS REG OK - FPGA 0x0006- REG VALUE 0x2D00
2020-10-28 16:22:00 - POWER ON - CURRENT OK - FPGA 6 - CURRENT VALUE 0
2020-10-28 16:22:00 - POWER ON - STATUS REG OK - FPGA 0x0007- REG VALUE 0x2D00
2020-10-28 16:22:00 - POWER ON - CURRENT OK - FPGA 7 - CURRENT VALUE 0
2020-10-28 16:22:02 - END POWER ON
    
```

HV SYSTEM

HV_STATE_CMD: MONITOR
HV_STATUS: HV OFF
HV STATE: HV OK

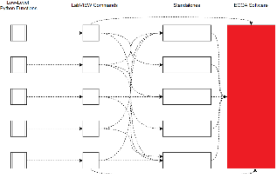
HV mon	HV set	I mon	I set	Vspeed	HV Status CH ver	HV ENABLED	CURR OK
0.032	850	0	1.42	4	HV OFF	CH	OK
0.009	850	0	1.42	4	HV OFF	CH	OK
-0.146	850	0	1.42	4	HV OFF	CH	OK
0.002	850	0	1.42	4	HV OFF	CH	OK
9999	9999	9999	9999	9999	DISABLED	CH	OK
9999	9999	9999	9999	9999	DISABLED	CH	OK
-9999	-9999	-9999	-9999	-9999	DISABLED	CH	OK
9999	9999	9999	9999	9999	DISABLED	CH	OK

HV LOG

```

2020-10-28 16:11:58 - DISCONNECT OLD CONNECTION
2020-10-28 16:11:59 - HV OLD CONNECTION - DISCONNECTED OK
2020-10-28 16:12:00 - START NEW HV CONNECTION
2020-10-28 16:12:01 - HV CONNECTED OK
2020-10-28 16:12:02 - START HV MONITOR OK
2020-10-28 16:12:04 - HV PAR SET OK
2020-10-28 16:12:05 - HV SET RAMP SPEED OK
2020-10-28 16:12:05 - START HV MONITOR OK
2020-10-28 16:12:07 - POWER OFF OK
2020-10-28 16:12:09 - START HV MONITOR OK
2020-10-28 16:14:24 - DISCONNECT OLD CONNECTION
2020-10-28 16:14:25 - HV OLD CONNECTION - DISCONNECTED OK
2020-10-28 16:14:26 - START NEW HV CONNECTION
2020-10-28 16:14:28 - HV CONNECTED OK
2020-10-28 16:14:28 - START HV MONITOR OK
2020-10-28 16:19:38 - POWER OFF OK
2020-10-28 16:19:40 - START HV MONITOR OK
2020-10-28 16:21:54 - DISCONNECT OLD CONNECTION
2020-10-28 16:21:55 - HV OLD CONNECTION - DISCONNECTED OK
2020-10-28 16:21:56 - START NEW HV CONNECTION
2020-10-28 16:21:57 - HV CONNECTED OK
2020-10-28 16:21:57 - START HV MONITOR OK
2020-10-28 16:22:44 - POWER OFF OK
2020-10-28 16:22:46 - START HV MONITOR OK
    
```

Elementary Cell Quality Assurance Software – Stage IV (3)



CHECK SETUP AND CONFIRM **SUBMIT SETUP**

param error

PARAM OK

SETUP_PARAM

auto setp sequence

S-Curve FAST	ENABLED
Check FEB curr CLARO comm	ENABLED
Check BaseBoard HV	ENABLED
SCAN PMTS	ENABLED
S-Curve FAST	ENABLED
Check HV EC+PMT	ENABLED
S-Curve HV OFF	ENABLED
Keep HV ON Night	ENABLED
THR scan	ENABLED
Dark counts OPT THR	ENABLED
Dark counts COM THR	ENABLED
SIN SCAN OPT THR	ENABLED
SIN SCAN COM THR	DISABLED
TEST FINISHED	ENABLED
EC CODE RECOVERY	DISABLED
EC CODE RECOVERY	DISABLED
EC CODE RECOVERY	DISABLED
EC CODE RECOVERY	DISABLED
EC CODE RECOVERY	DISABLED

EC TYPE

R

INIT SYS CTL

python DEAMON source file (with absolute path)
/home/labo/ECQA/LabVIEW/SysCmd/syscmd_labview_interface.py

NET PARAM

ipaddr (192.168.1.200)
192.168.1.201

port (15) sysport (1) timeout python
15 1 5

sysaddr (144)
145

Check FEB curr and CLARO com

daq_statusREG_atPowerON
D00

currTHR_atPowerON
35

CLARO CFG LOW THR
CH cfg: 000
COM BYTE: 0

QUERY_statusREG_UNCONF
2D00

CLARO CFG HIGH THR
CH cfg: 000
COM BYTE: 0

QUERY_statusREG_CONF
2D00

CLARO CFG DEFAULT
CH cfg: 320
COM BYTE: 8

ADC_ref_before_CFG	ADC_ref_after_CFG
2350	2350
2350	2350
2350	2350
1250	1250
2350	2350
40	300
850	850
850	850

HV general

ISEG IP Address
192.168.1.100

RampUP V/s
4

Current Limit RAMP (mA)
2

Current Limit (mA)
1.418

HV check EC+PMT (MB3)

HV value (V)
1000

Curr Limit (mA)
1.418

CLARO CFG
CH cfg: 320
COM BYTE: 8

T/H rpi monitor

IP rpi
192.168.1.203

tcp/ip port
5000

Time Meas (s)
10

HV/THR SCAN (MB4)

START THR	START HV
0	1000
STOP THR	STOP HV
63	1000
STEP THR	STEP HV
1	50
Curr Limit (A) 1.418	

CLARO CFG
CH cfg: 320
COM BYTE: 8

LED SETUP

N Pulses (k)
100

Freq
100

PMT LED ENABLE
[ON]

HV stability

HV value (V)
1050

Curr Limit (mA)
1.492

Time (h)
8

OPT THR config

Use always this opt thr
[ON]

HV
1000

Dark Count Rate

HV (V)
1000

Time (sec)
100

CLARO CFG
CH cfg: 307
COM BYTE: 8

S-Curve

N PULSES
1000

778
788
798
2858
2868
2878

DAC MIN: 0
DAC MAX: 600
DACSTEP: 1
MODE: 4
MASK: 255
HV (V): 1000

SIN TEST

Use only first HV
[ON]

HV STEP

1000
950
900
850
0

CLARO COM CFG
CH cfg: 320
COM BYTE: 8

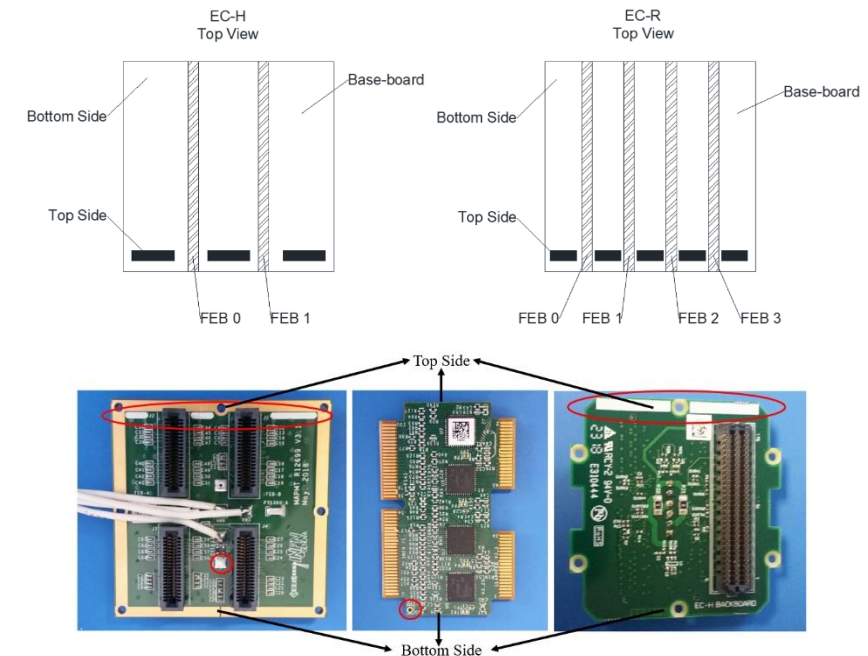
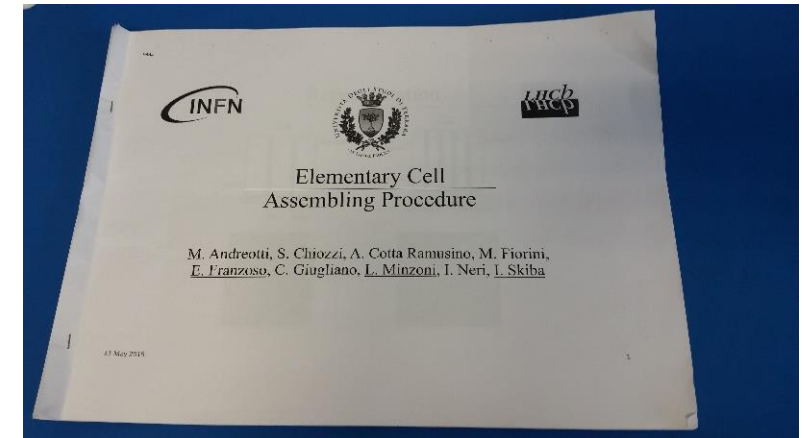
Elementary Cell Quality Assurance Protocol and Assembling Manual (1)

Author: Igor Ślęzyk

- Test protocol – a complete protocol used for the ECQA procedure
- Assembling manual – a complete guide to properly assembly ECs

Test protocol for EC QA version 4
[in blue: parameters to be written to the Data Base and to be stored on disk]

- 1) Mount 4 EC without PMTs on the panel (in the afternoon)
- 2) Check FEB currents and communication to the CLAROs
 - a. Power on
 - b. Read currents
 - c. Send a POR command (and SEU counter clear) and read-back registers to see if they are all 0 → if you don't have all 0 STOP
 - d. Send a configuration to all channels and to the common part of the register (configuration to see that all channels are on and alive, to see noise) → one with negative threshold and one with very high threshold
 - e. Data output:
 - i. QUERY results for all FEB_DB
 - ii. Measure currents for each FEB pair, temperatures from all PTCs
 - iii. 128-bit CFG register for all CLAROs after POR and SEU counter reset (all bits in the 128-bit register should be 0)
 - iv. 128-bit CFG register for all CLAROs after ACFG command
- 3) Check HV stability of Base-Board
 - a. Close the dark box (safety interlock) and set HV to 1150 V (use ramp up rate of 40 V/s)
 - b. Measure current consumption of Base-Boards with 1000 V applied voltage
 - c. Check if currents are OK for 1 hour (extract BB resistance from DB and compare to the measured current value)
 - d. Set two current limits: one higher value for ramp-up, a lower value (after ramp up) just above the expected current consumption (calculated from DB)
 - e. Check possible CLARO activity due to sparks or other effects
 - f. Turn HV OFF
- 4) Mount PMTs on the ECs and close dark box
 - a. Check visually if PMTs are mounted at an angle, if they touch → use the "Padova" or CERN mask to check distance between and the planarity between them
- 5) Set HV to 1000 V (40 V/s ramp-up)
 - a. Check if currents are OK (set current limit close to the expected value)
 - i. Measure currents of Base-Boards + PMTs with 1000 V applied voltage
 - b. Check if all PMT channels are alive with LED run (HV=1000V, threshold 7, 100k triggers)
 - c. Make a quick DCR measurement to look for noisy or dead pixels
- 6) S-curve check on all CLAROs before dark count (HV OFF)
 - a. Make measurements for 3 different thresholds and extract linearity curve
 - b. (to be checked if S-curves with HV ON give same results: in this case move this test during the night)
 - c. Make data analysis to extract useful parameters (store in the DB: 3 transition points and sigma per channel, for 3 different threshold values)
 - i. Save complete raw data for all S-curves (ASCII files) and store on disk
 - ii. Save to the DB the transition points and sigmas for all S-curves
- 7) Dark counts
 - a. Keep HV ON at 1000 V all night
 - b. Measurement of DCR in the morning (threshold 7, time duration ~10 min) → run (compare with the DCR measured in PDQA → extract from DB)
- 8) Threshold scan
 - a. Put HV at 1100 V for 10 minutes (monitor currents), then go back to 1000V
 - b. Scan threshold from 63 to ~20 (or lower), with offset bit enabled and attenuation=0 (to see the pedestal)
 - c. For each threshold value we should collect about 100k triggers (to be checked: start with 100 kHz and decrease in case of issues)
 - d. Make 4 threshold scans with different HV settings: 1000 V, 950 V, 900 V and 850 V
 - e. Make data analysis to extract the "threshold working point"
 - i. Working point is determined looking for the transition from pedestal in the measurement with offset=1, and adding 5 threshold steps
 - ii. Save raw data for all threshold scans to disk
 - iii. Save optimized thresholds to the DB
- 9) Set the "working point parameters" (threshold/offset/attenuation) for each individual CLARO channel
 - a. Load a "configuration file" with the values determined in the previous step to all CLARO channels
 - b. Make DCR measurement to look for noisy pixels
 - i. Save DCR measurement at 1000 V with optimized thresholds
 - c. Make LED run to see that uniformity is good on all pixels
- 10) Make SIN measurement
 - a. Count pulses in 2 different time windows relative to the LED trigger time: one "in-time" and one "delayed" window
 - i. Width of the windows and delay relative to the trigger are still to be defined
 - ii. LED repetition rate to be carefully defined (wait at least 3 microsec from one LED pulse and the next)
 - iii. Save raw data to disk
 - iv. Extract SIN intensity for each pixel and save to DB
- 11) Acceptance/rejection of individual ECs
 - a. Manual operation from the operator, based on summary plots and data
 - b. Load the relevant information in the DB

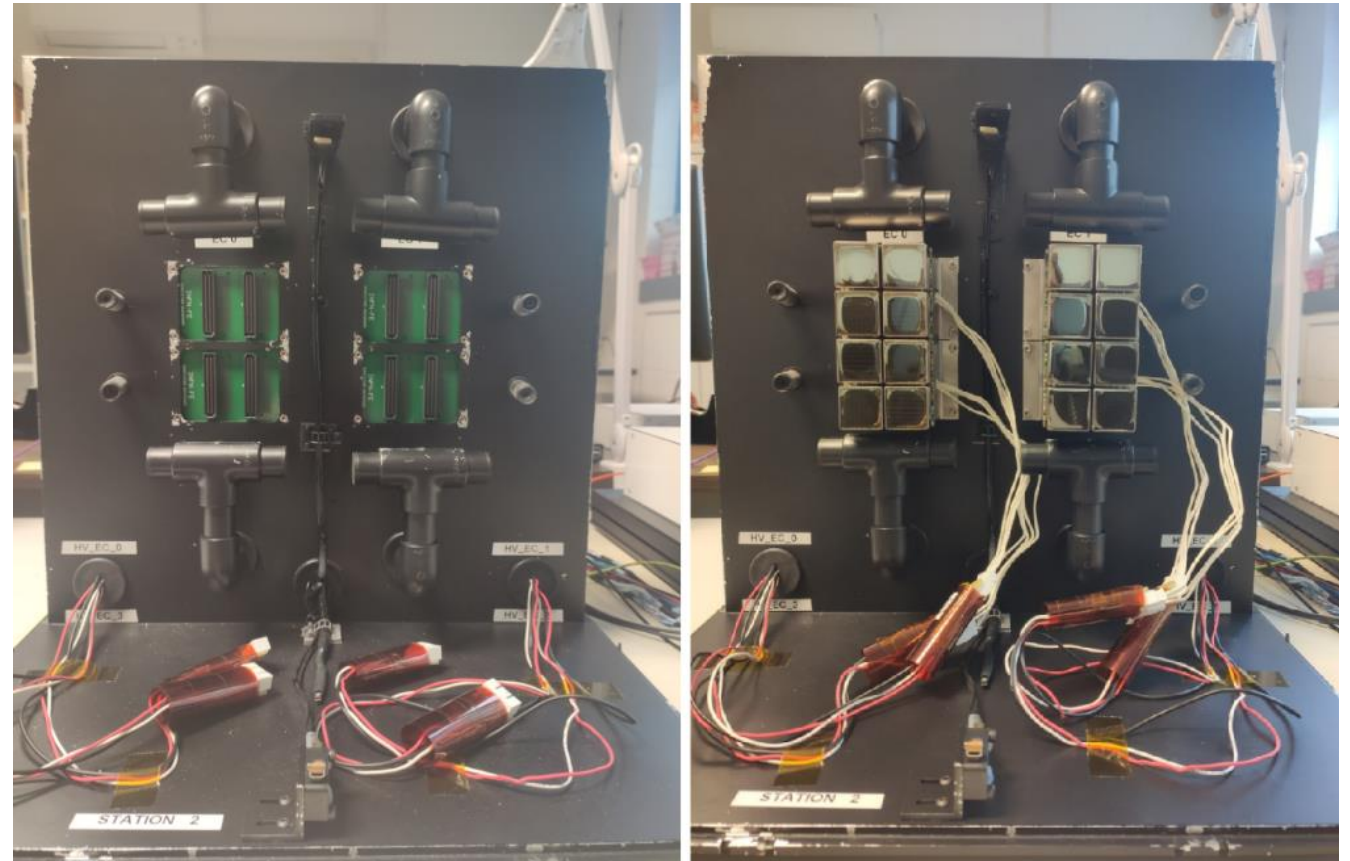


Elementary Cell Quality Assurance Protocol and Assembling Manual (2)

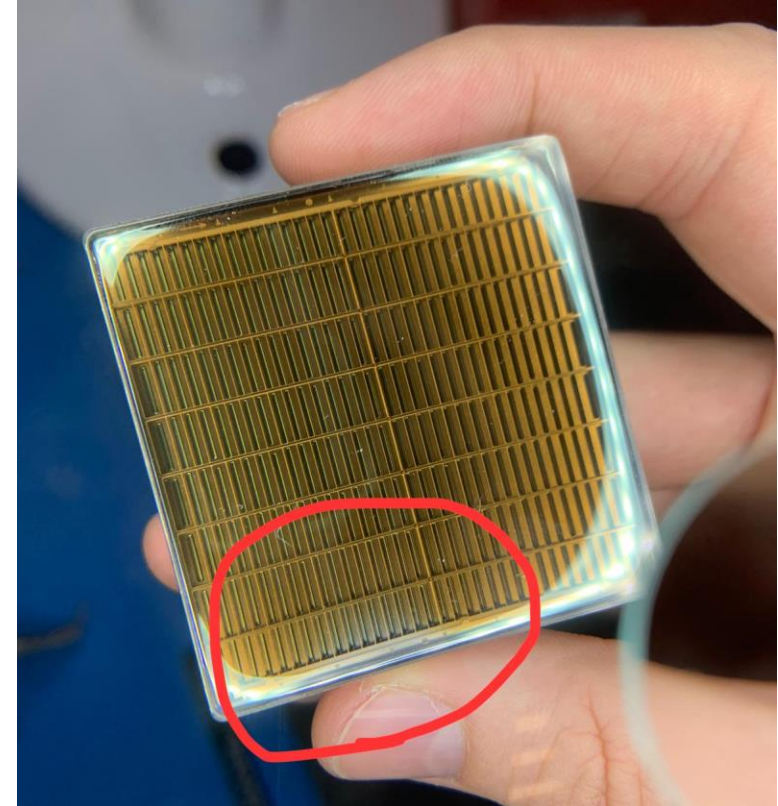
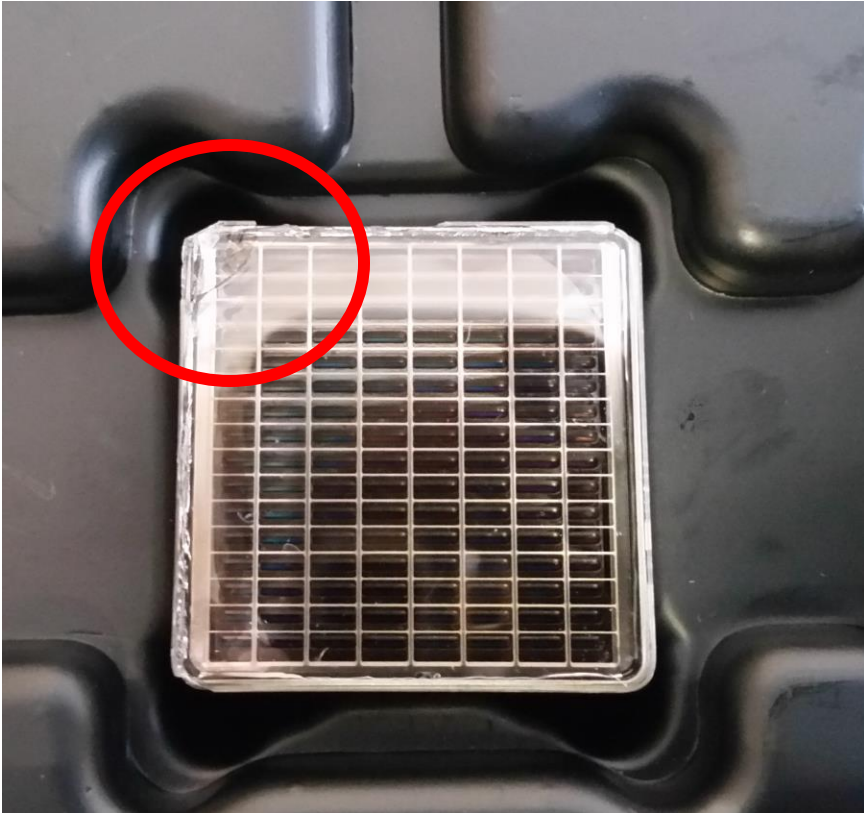
Author: Igor Ślęzyk

Procedure:

- Preparation of readout electronics for assembly
- Quick response (QR) code scanning
- Assembly – ECs without MaPMTs
- Mounting of ECs to test stations
- Test measurements on FE read-out electronics
- Preparation of MaPMTs according to grouping schemes
- Installation of MaPMTs with QR code scanning
- MaPMTs training – 10 hours
- Test measurements on MaPMTs
- Revision of obtained data
- Preparation of tested ECs for shipments to CERN



Elementary Cell Quality Assurance Mistakes Were Made



Elementary Cell Quality Assurance Offline Data Analysis

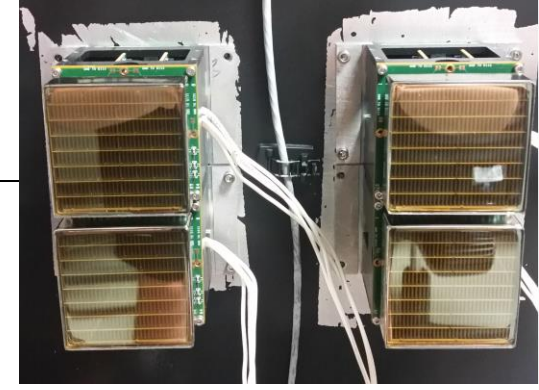
Authors: Igor Ślazyk
Luca Minzoni
Edoardo Franzoso

- Written in Python and C++
- [Essential for revising obtained results](#)
- Electronic (CLARO channel) and optical (MAPMT) mapping correlation

Analyses:

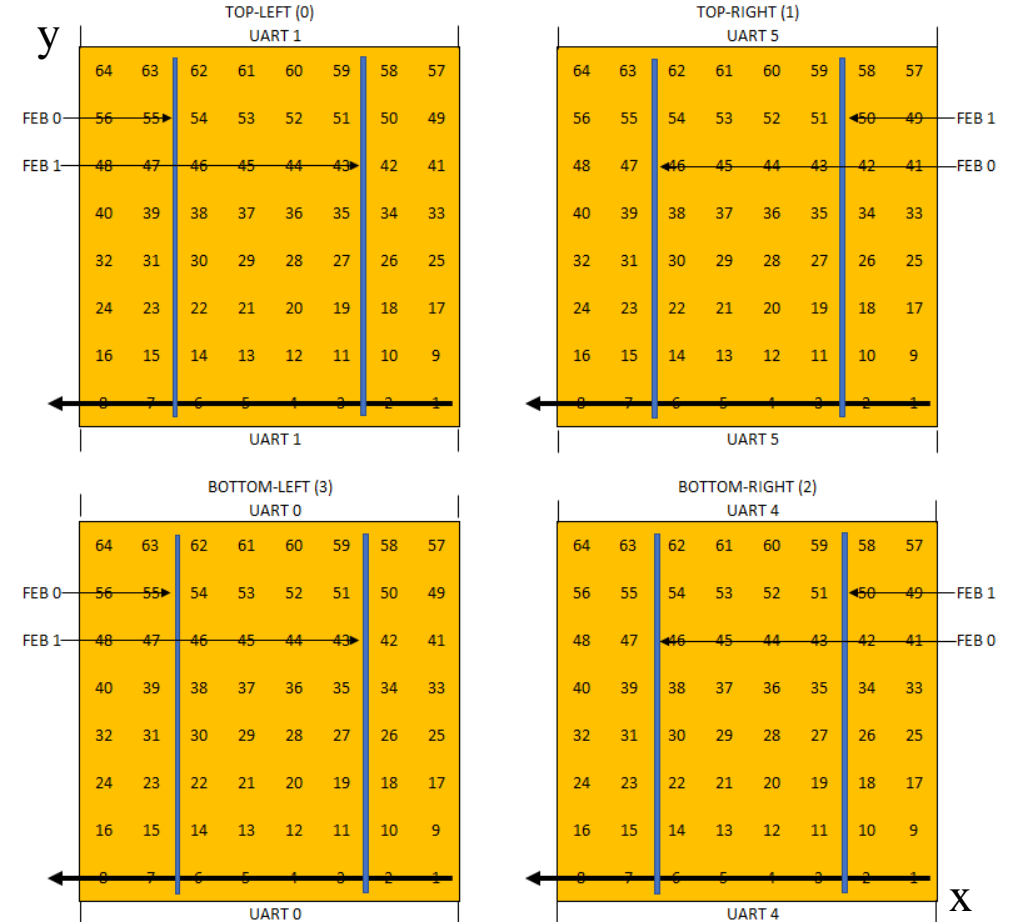
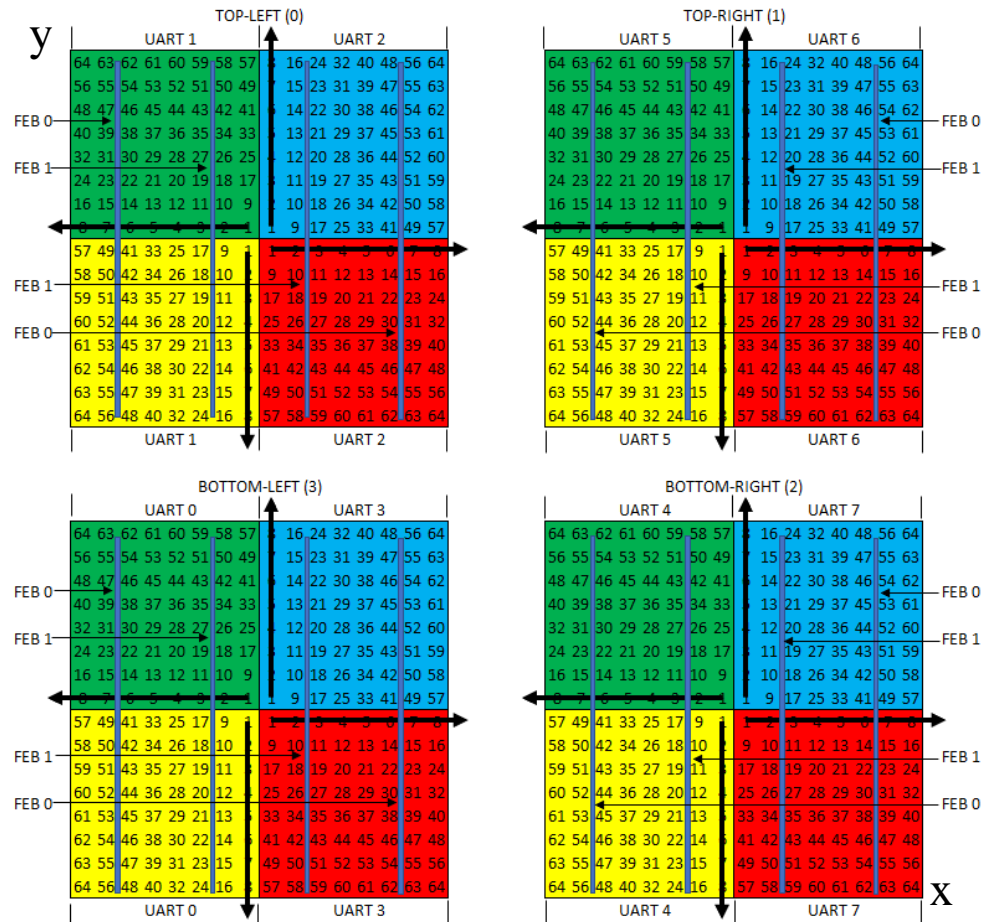
- Digital-to-Analog Converter (**DAC**) Scan
- Threshold (**THR**) Scan,
- Dark Count Rate (**DCR**),
- Signal Induced Noise (**SIN**).

Elementary Cell Quality Assurance Mapping (1)



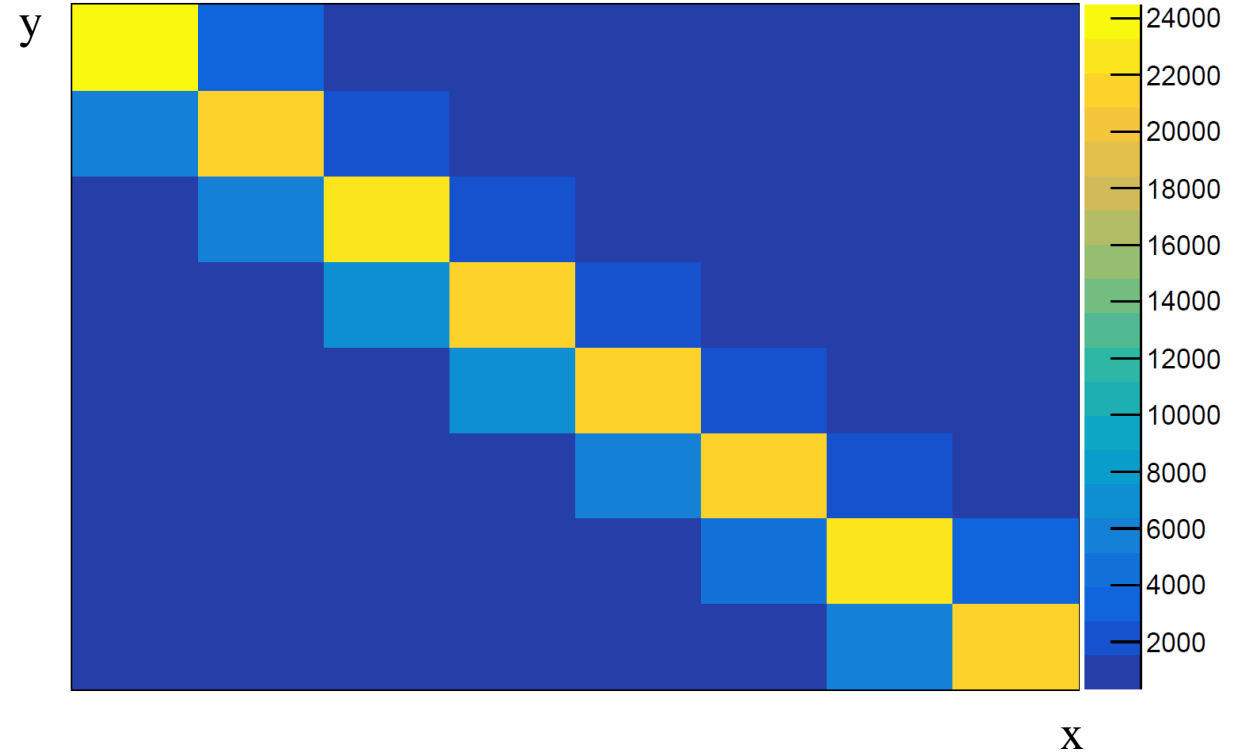
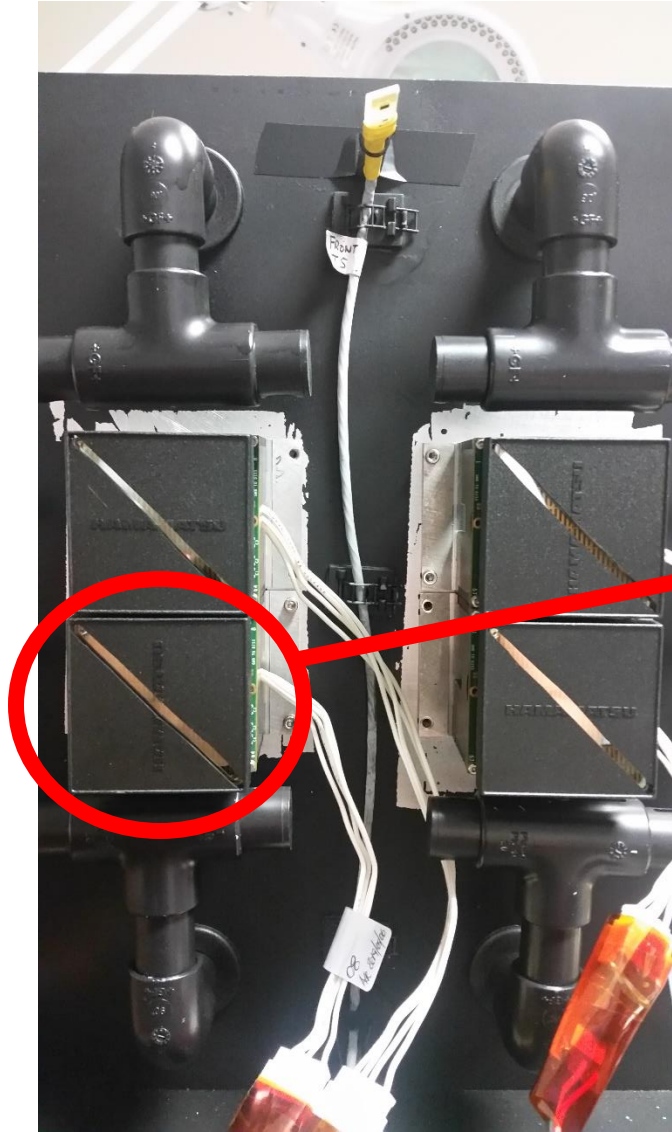
R-type load (4 R-type ECs)

H-type load (4 H-type ECs)



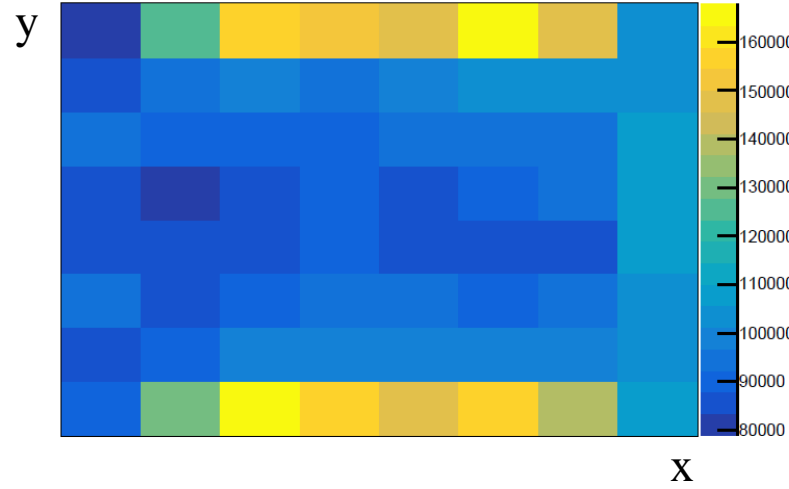
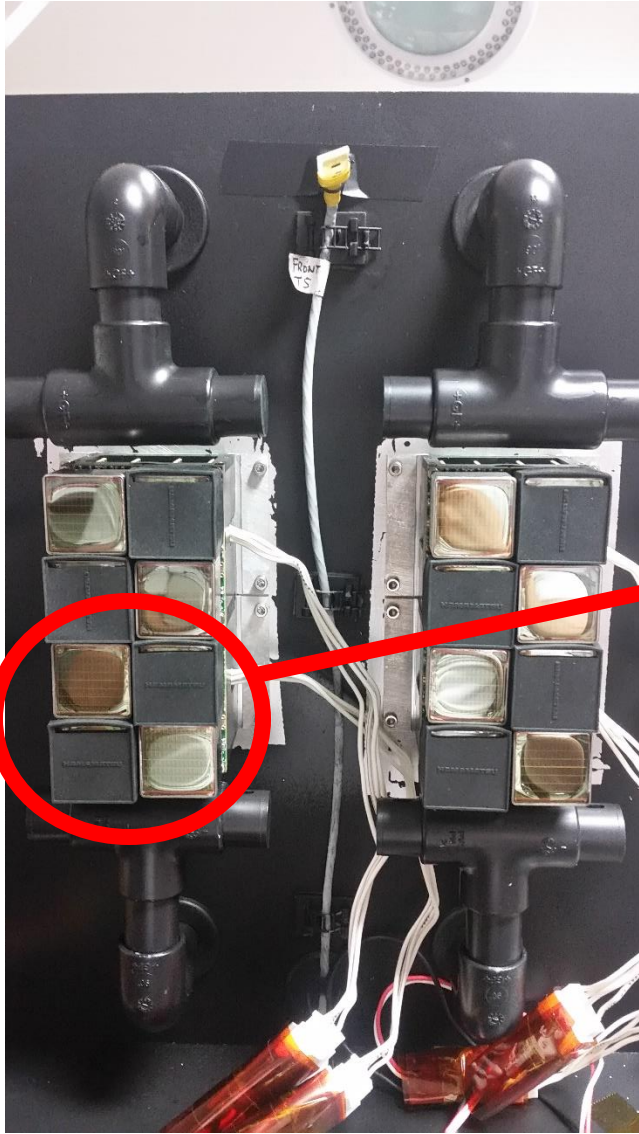
Elementary Cell Quality Assurance Mapping (3)

Author: Igor Ślęzyk



Elementary Cell Quality Assurance Mapping (2)

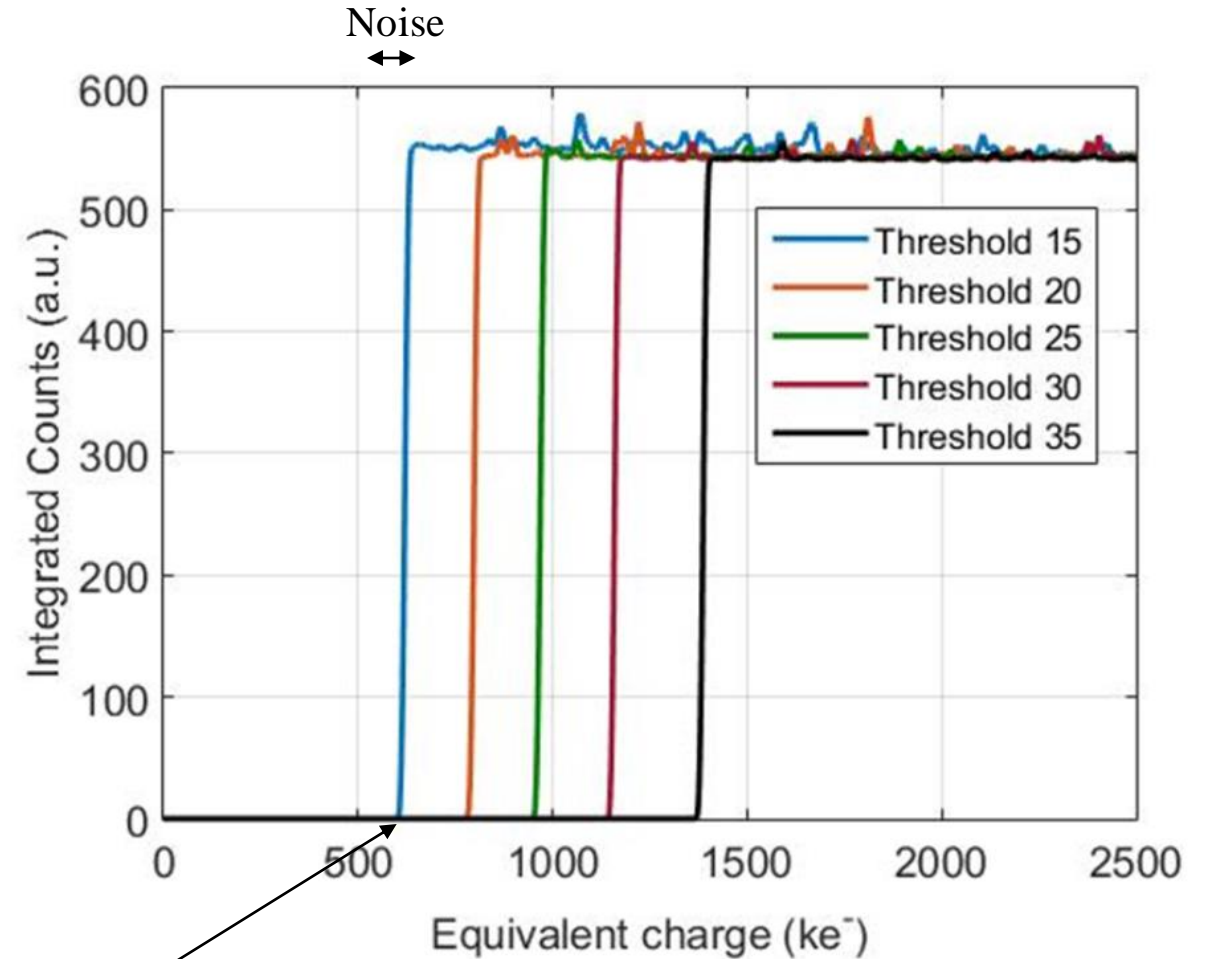
Author: Igor Ślęzyk



Elementary Cell Quality Assurance

Digital-to-Analog Converter Scan (1)

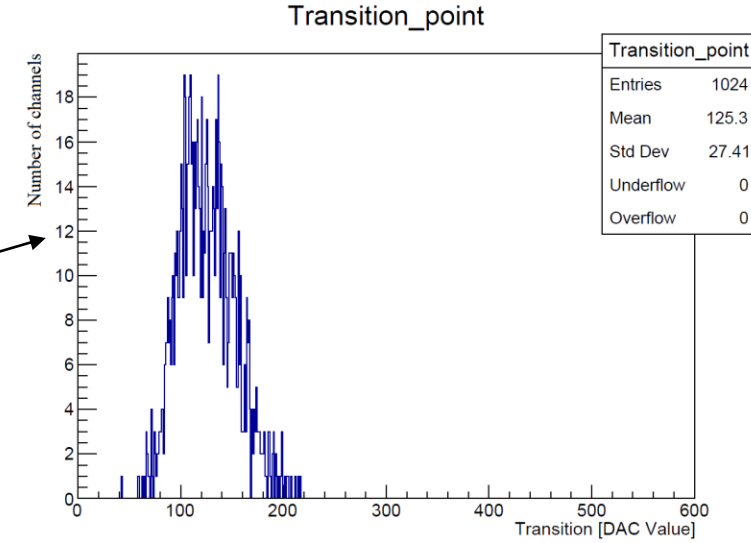
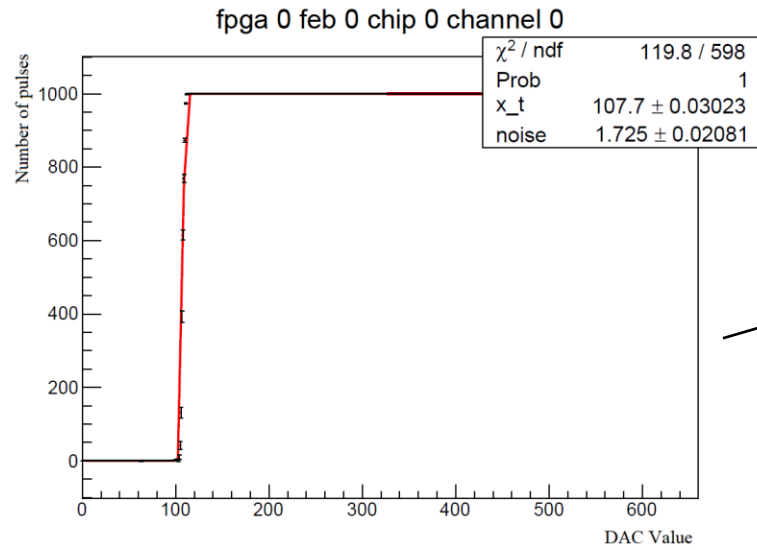
- Used for the calibration of the CLARO channels
- Known charge Q_{inj} injected at fixed threshold
$$Q_{inj} = DAC_{step} \times 1.22 \text{ mV} \times 640\text{fF} \cong DAC_{step} \times 4.874 \text{ ke}^-$$
- Amplitude of the signal gradually increases
- If the charge is lower than the threshold \rightarrow output 0
- If the charge is higher than the threshold \rightarrow output 1
- Parameters of interest:
 - Transition point x_{tr}
 - Noise σ
- Fitted using translated error function: $f(x) = \frac{1}{2} \left[1 + \text{erf} \left(\frac{x - x_{tr}}{\sigma} \right) \right]$
- DAC scan also referred as S-Curve test



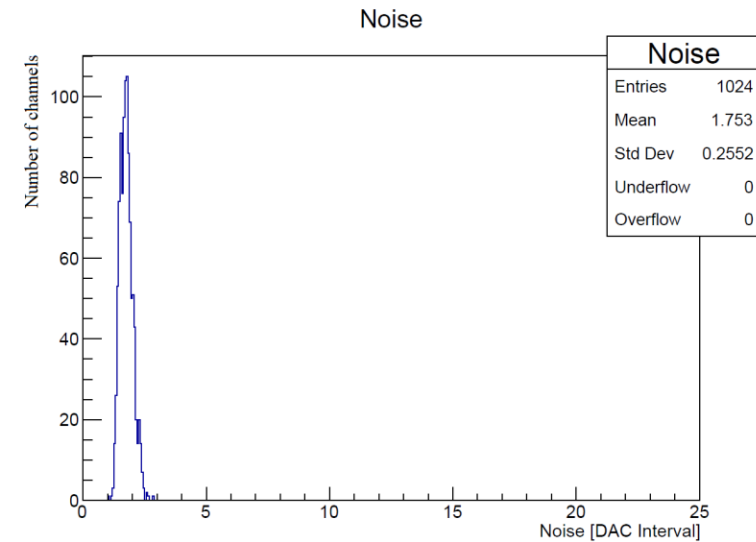
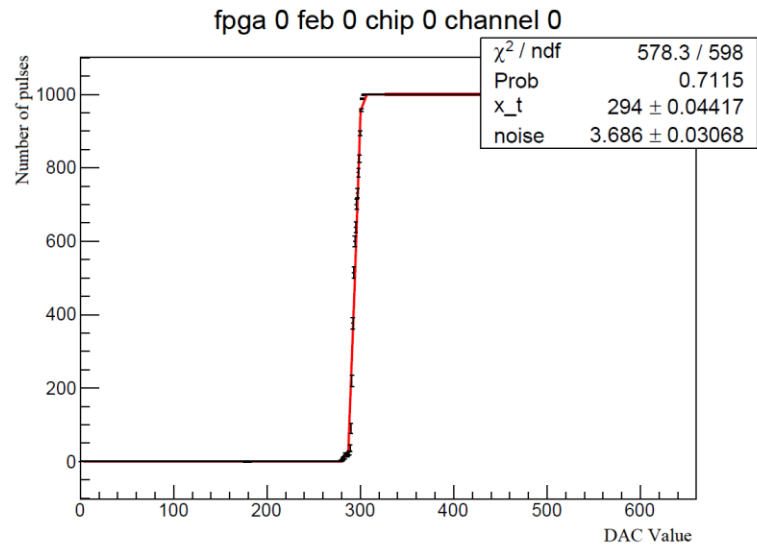
Elementary Cell Quality Assurance

Digital-to-Analog Converter Scan (2)

Threshold 10



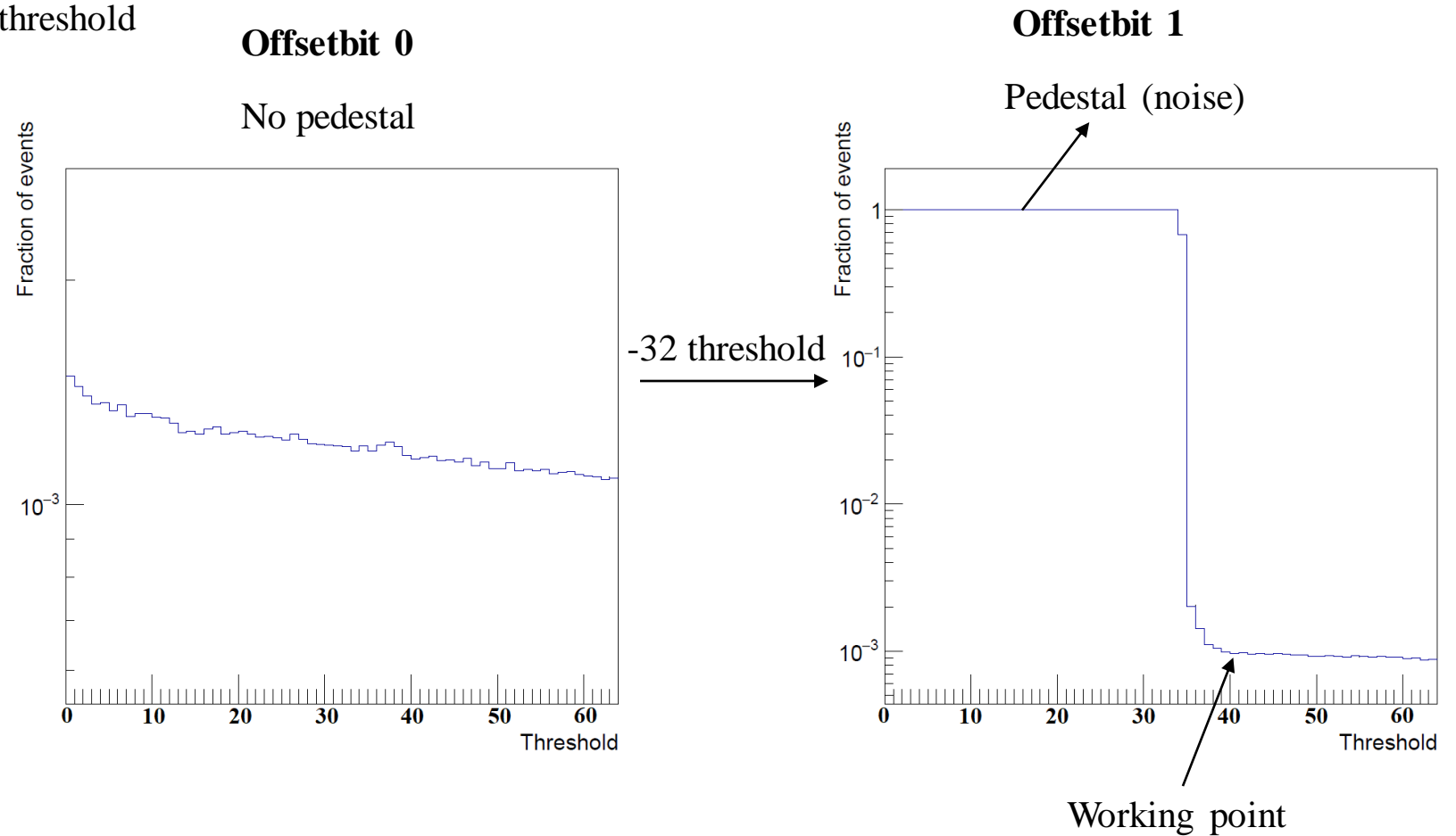
Threshold 62



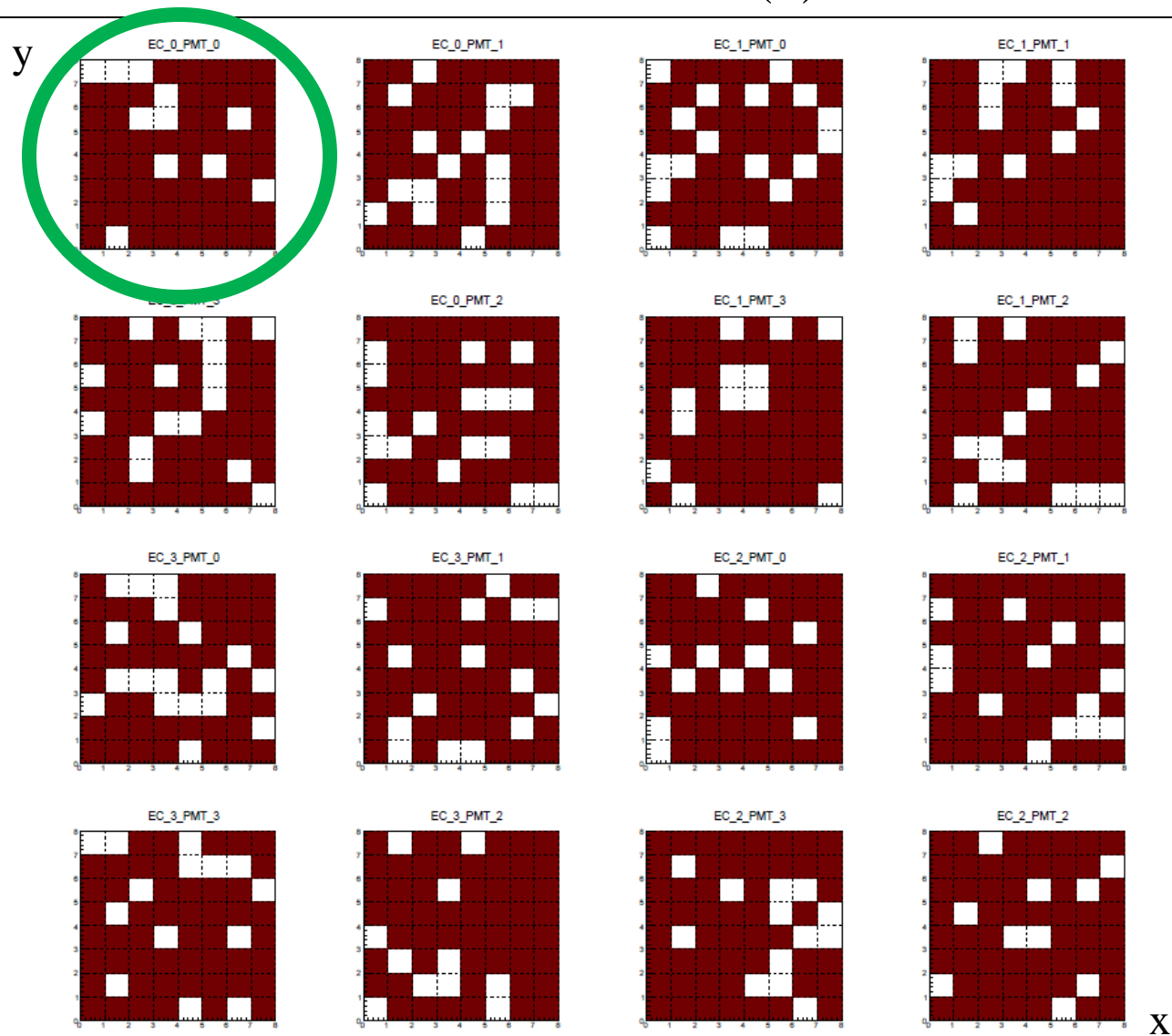
Elementary Cell Quality Assurance

Threshold Scan (1)

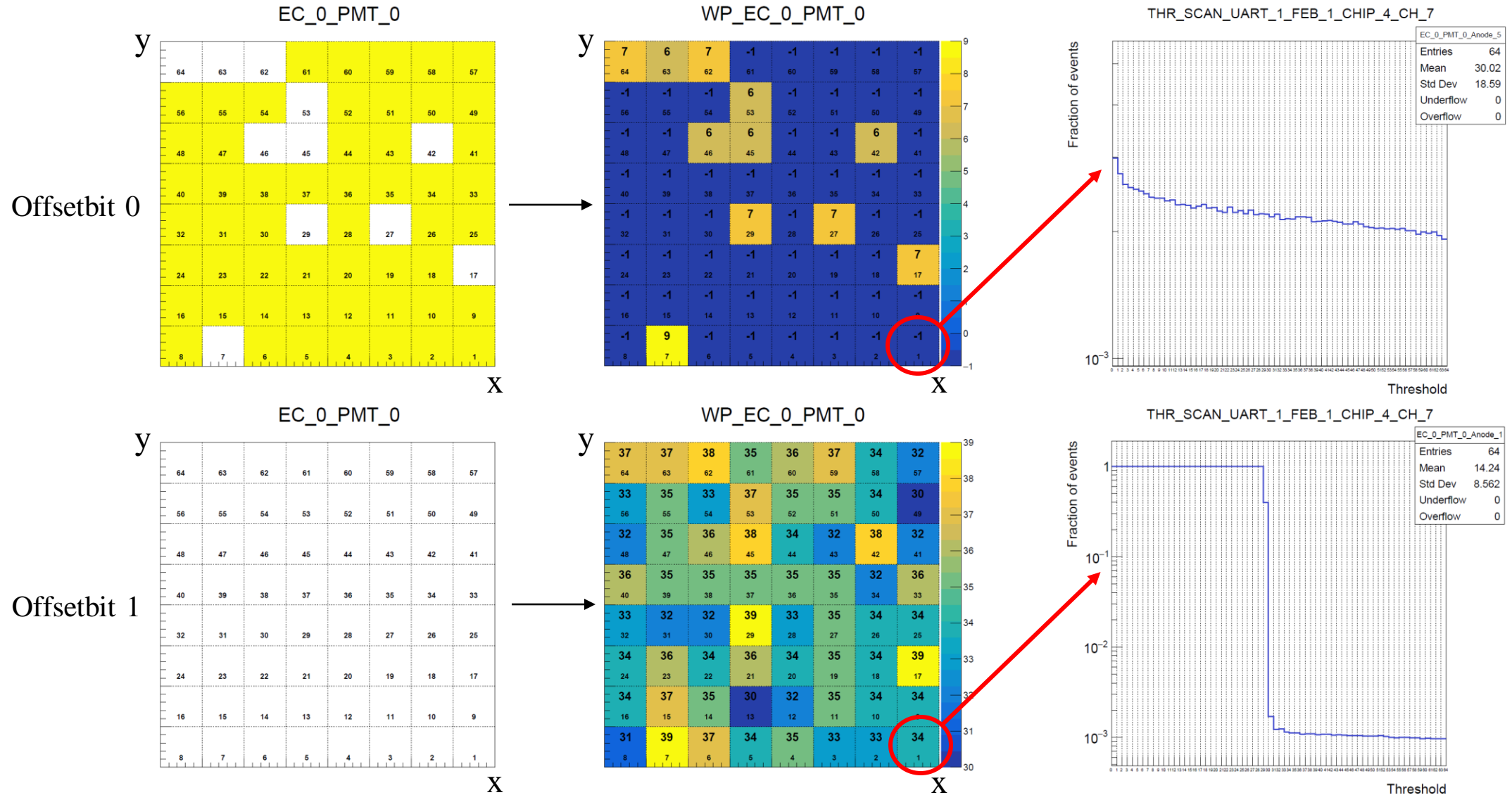
- Used for the calibration of the MaPMTs anodes
- Known charge Q_{inj} injected at decreasing threshold
- Amplitude of the signal fixed
- Distribution of above-threshold events
- Parameters of interest:
 - Working point w_p
- At certain threshold (working point) the noise is well separated from the signal
- Offsetbit 0 and 1 – shifts threshold by -32



Elementary Cell Quality Assurance Threshold Scan (2)



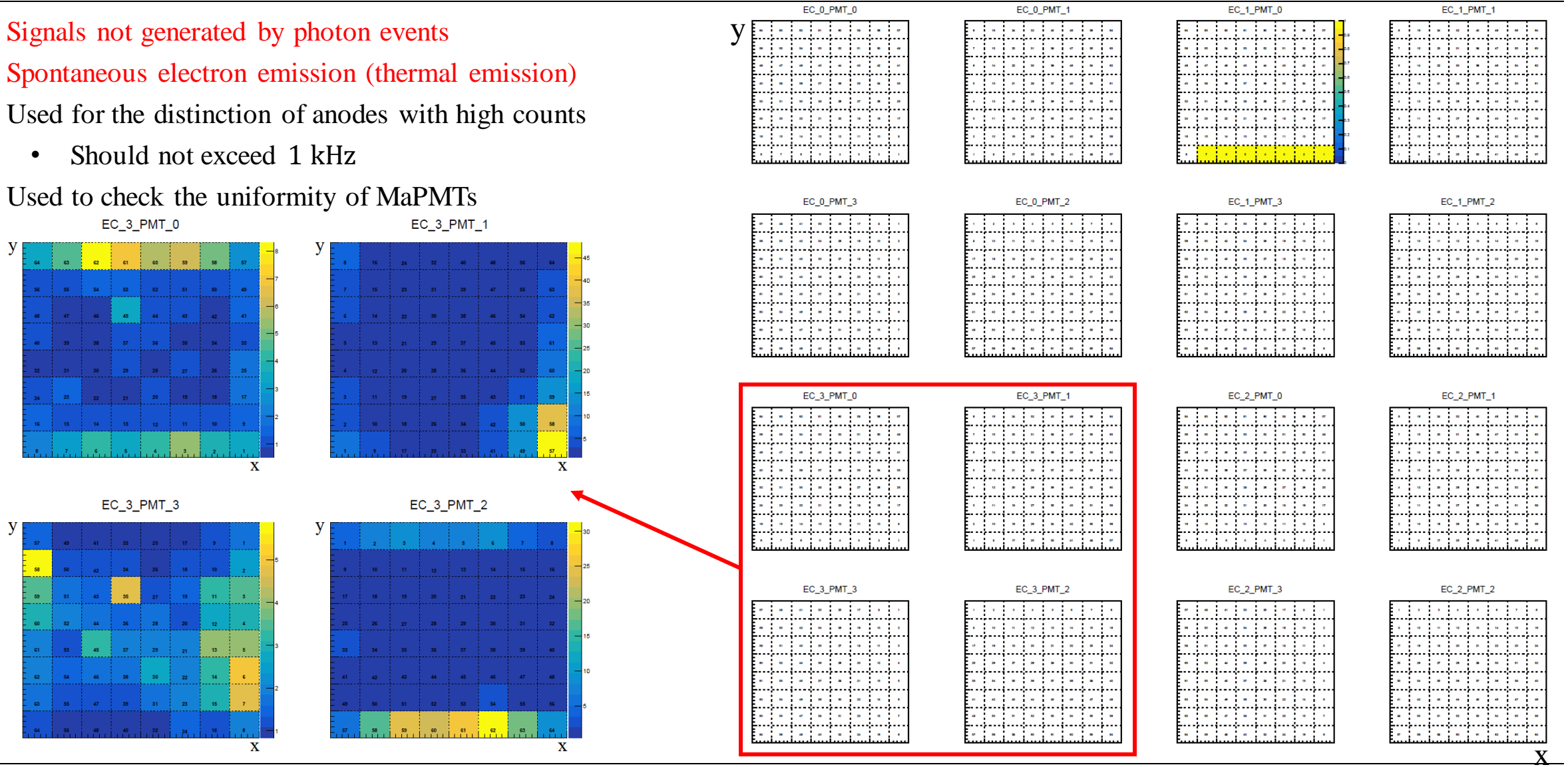
Elementary Cell Quality Assurance Threshold Scan (3)



Elementary Cell Quality Assurance

Dark Count Rate

- Signals not generated by photon events
- Spontaneous electron emission (thermal emission)
- Used for the distinction of anodes with high counts
 - Should not exceed 1 kHz
- Used to check the uniformity of MaPMTs



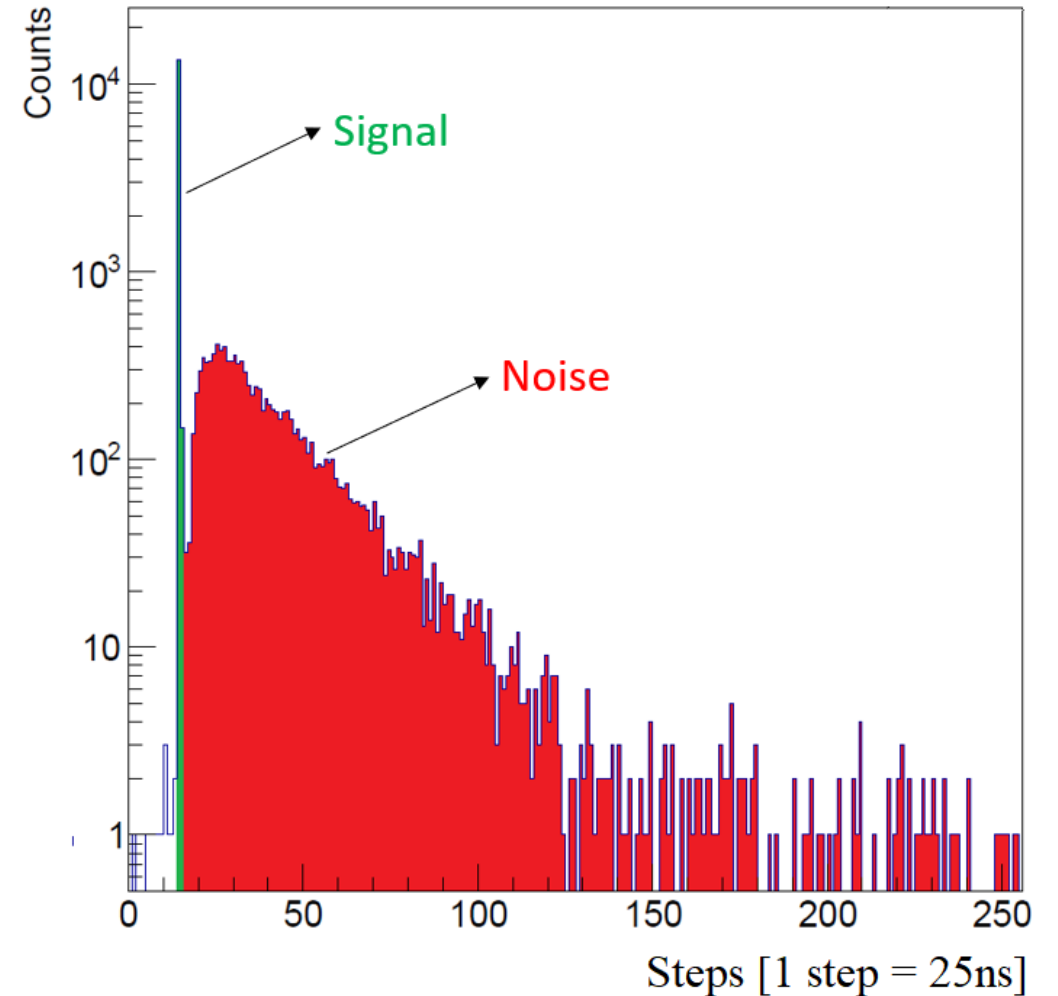
Elementary Cell Quality Assurance

Signal Induced Noise (1)

- Signals after the true signal
- Also referred as after-pulses
- Undesirable effect
- SIN step 14 – 15 [325 – 350ns] → signal
- SIN step 16 – 255 (350 – 6.375μs] → noise

Parameters of interest:

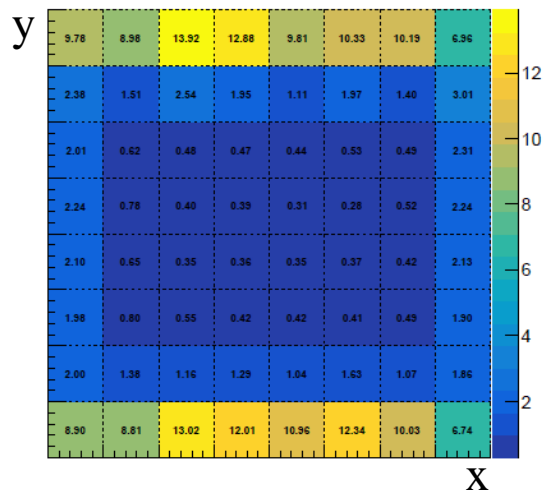
- $SIN_Fraction = \frac{noise}{signal+noise}$
- $S/N\ Ratio = \frac{signal}{noise}$
- For R-type ECs:
 - Hamamatsu introduced almost 200 so-called SIN-less MaPMTs
 - Since then, all other MaPMTs are referred as SIN-affected MaPMTs



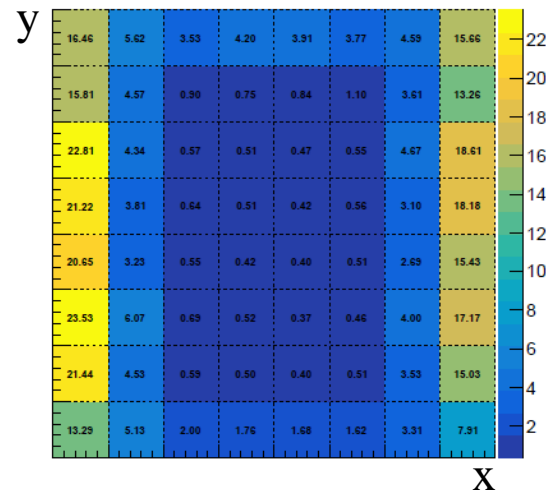
Elementary Cell Quality Assurance

Signal Induced Noise (2)

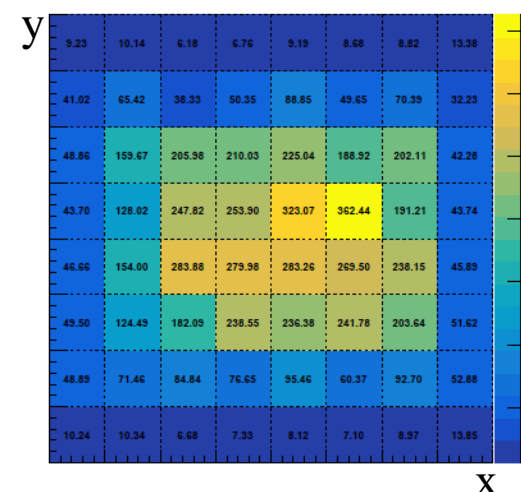
PMT A - SIN Fraction [%]



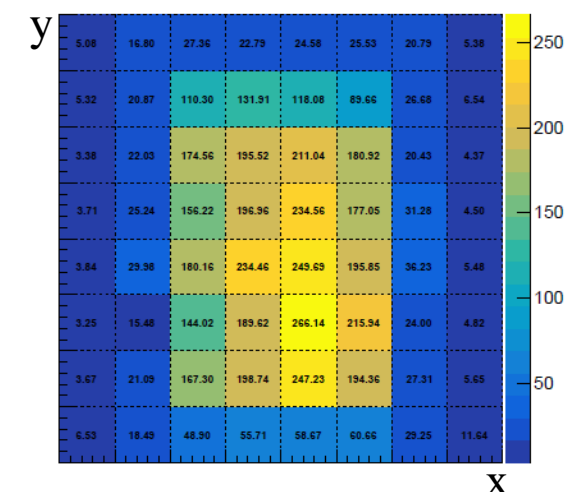
PMT B - SIN Fraction [%]



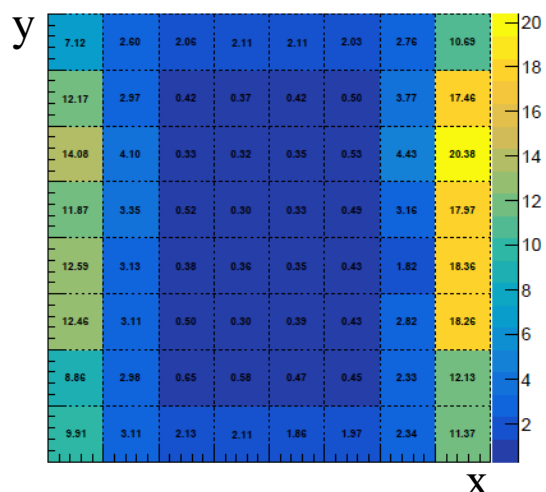
PMT A - S/N Ratio



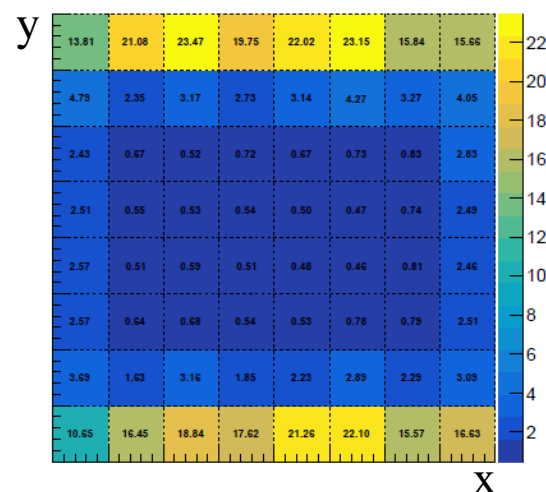
PMT B - S/N Ratio



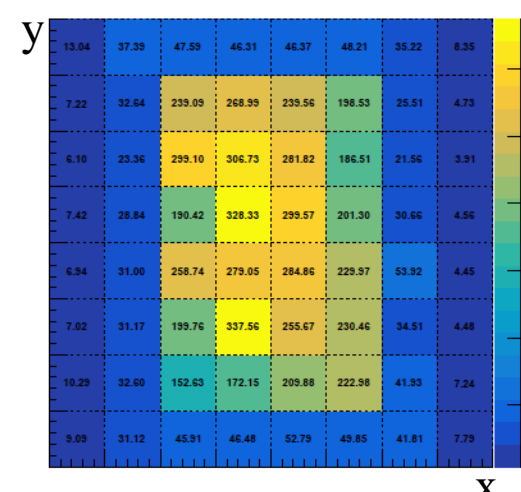
PMT D - SIN Fraction [%]



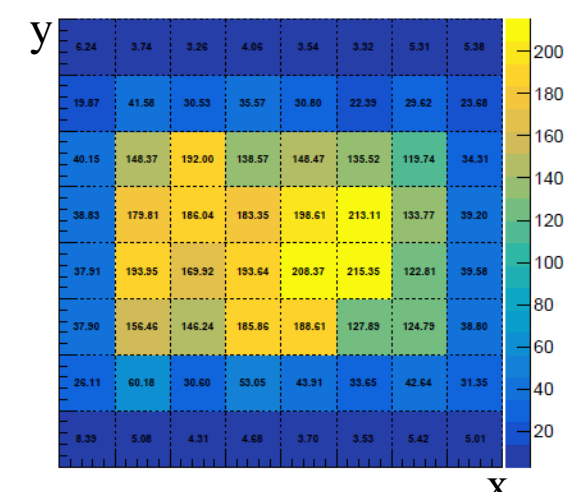
PMT C - SIN Fraction [%]



PMT D - S/N Ratio



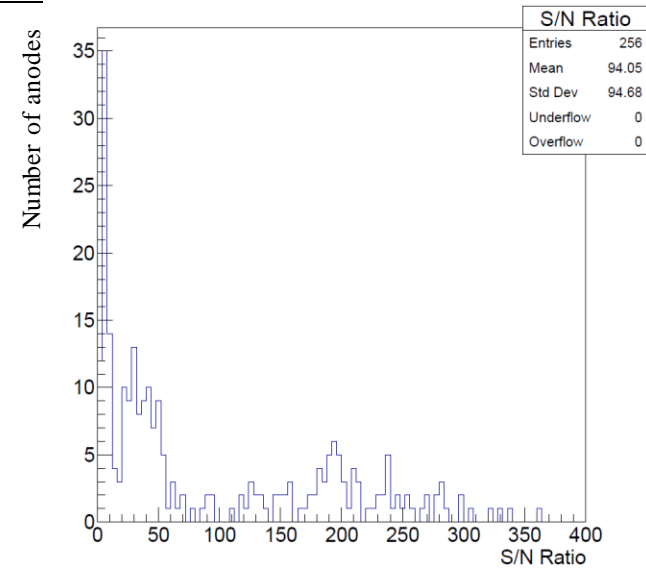
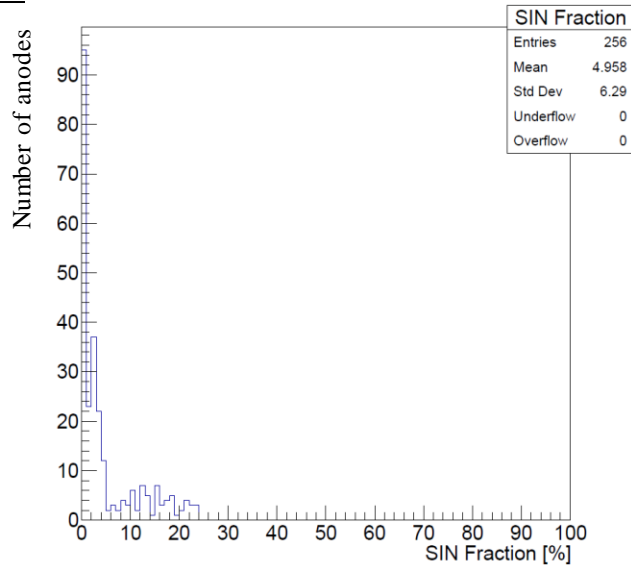
PMT C - S/N Ratio



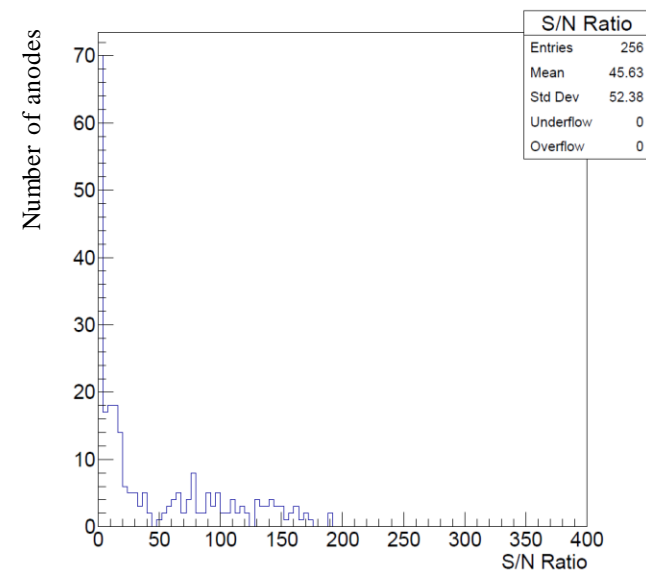
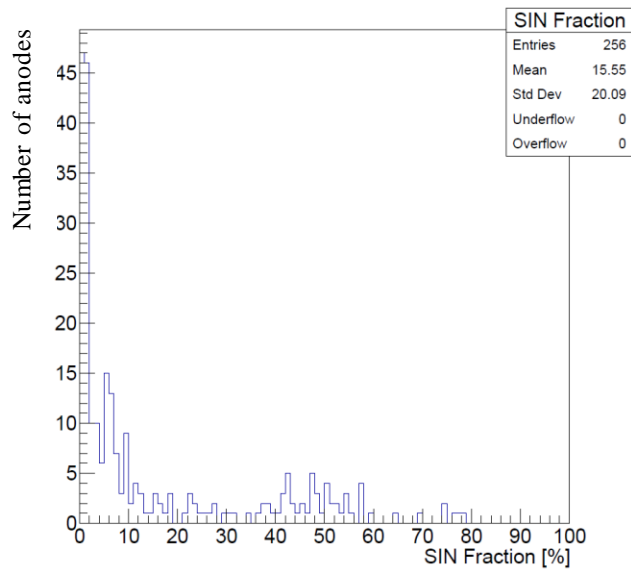
Elementary Cell Quality Assurance

Signal Induced Noise (3)

SIN-less EC



SIN-affected EC

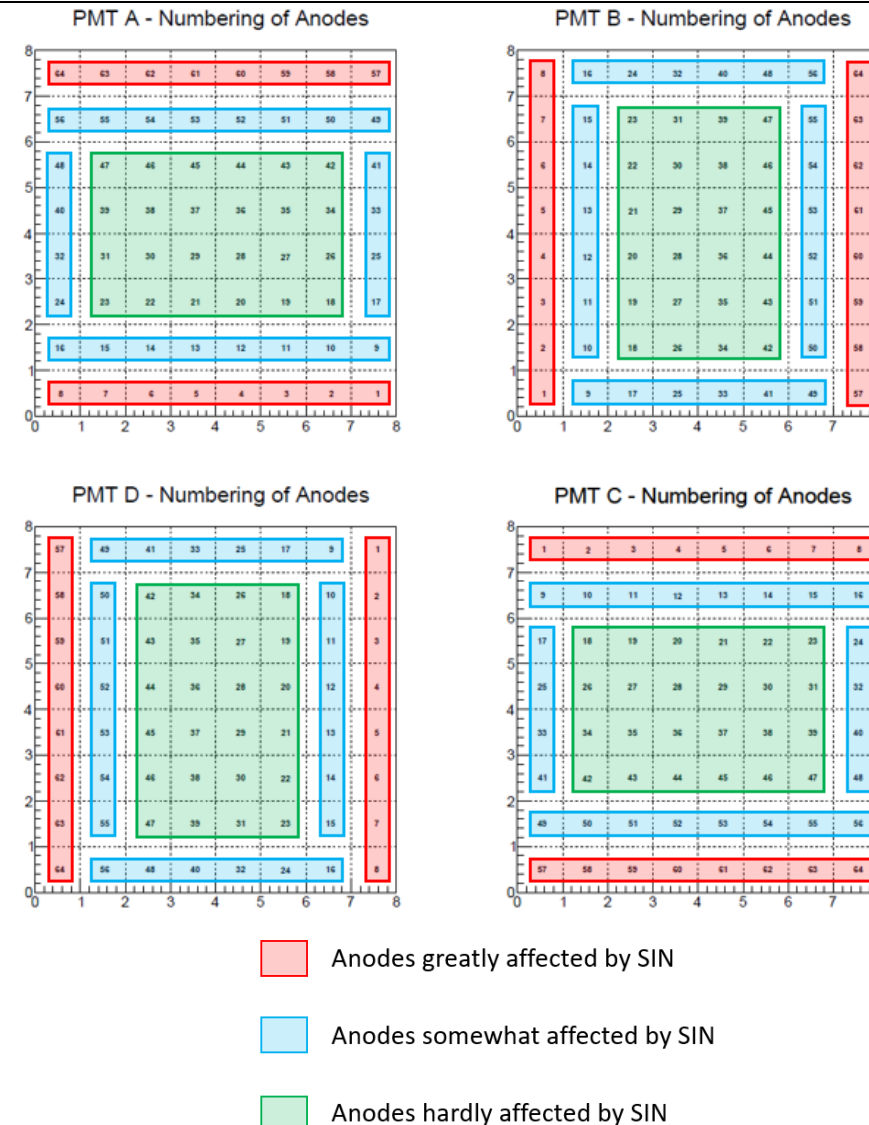


Elementary Cell Quality Assurance

Signal Induced Noise (4)

12 SIN-affected ECs and 12 SIN-less ECs compared (48 PMTs – 3072 Anodes).

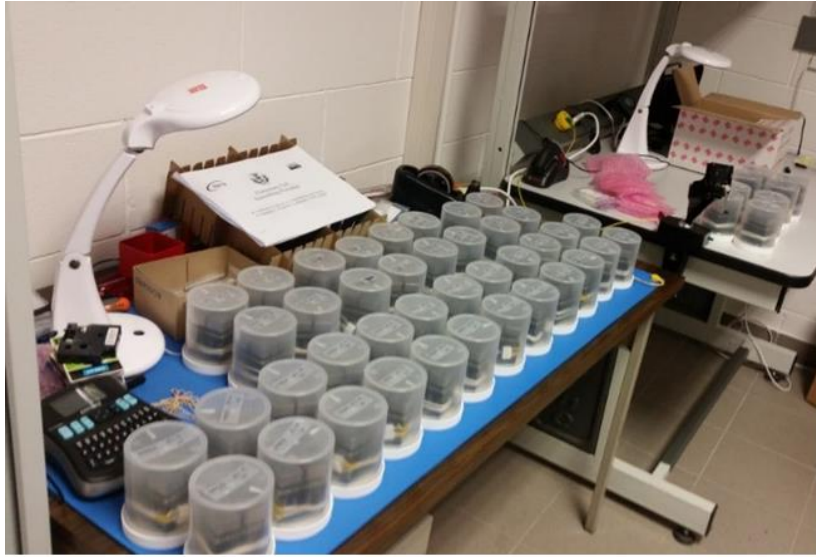
- Average SIN Fraction of SIN-less ECs compared to SIN-affected ECs is:
 - 52% lower (anodes hardly affected)
 - 64% lower (anodes somewhat affected)
 - 63% lower (anodes greatly affected)
 - 63% lower (all anodes)
- Average S/N Ratio of SIN-less ECs compared to SIN-affected ECs is:
 - 2 times higher (anodes hardly affected)
 - 2.25 times higher (anodes somewhat affected)
 - 3.95 times higher (anodes greatly affected)
 - 2.05 times higher (all anodes)



- **SIN greatly reduced in the SIN-less ECs**
- Advisable to be used in the regions with highest occupancy

Elementary Cell Quality Assurance Shipments

Author: Igor Ślęzyk



Conclusions

The ECQA in Ferrara finished successfully

- Experimental test setup proved to be reliable
- Fully automated software developed
- Quality control measurements fully completed
- Offline analysis scripts implemented in the final software
- Protocols and manuals produced
- SIN in SIN-less ECs proven to be substantially decreased
- Quality assurance results sent to CERN's database

- 581 ECs tested and sent to CERN (~55%):
 - 387 ECs of Type-R (~58%)
 - 194 ECs of Type-H (~51%)

- **RICH detectors should perform great in the future runs!**

Thank you for your attention



My Contribution

- Development and optimization of the test setup for quality control of the Elementary Cells
- Software development of the automated software for the Elementary Cells quality assurance
 - Python-LabVIEW Interface (Stage II)
 - LabVIEW Commands (Stage II)
 - Temperature and Humidity Read-Out Software (Stage II)
 - Standalones (Stage III)
 - Data analysis scripts (Stage III)
- Preparation of the test protocol and Elementary Cell assembly manual
- Hardware testing and assembly of the Elementary Cells
- Mapping tests
- Quality control measurements of the Elementary Cells
- Data analysis of the Elementary Cells quality assurance (SIN-less ECs)
- Minor data analysis on the example of the $B_s^0 \rightarrow D_s^\mp K^\pm$ decays
- Shipments to CERN

Backup

The LHCb Experiment at CERN Upgrade (2)

Reasons for the upgrade:

- More data to further challenge theoretical predictions
- Expose of detectors to radiation damage over years
- Bottleneck of Level-0 hardware trigger (1.1 MHz)
- Change in parameters → new geometry

LHCb Upgrade:

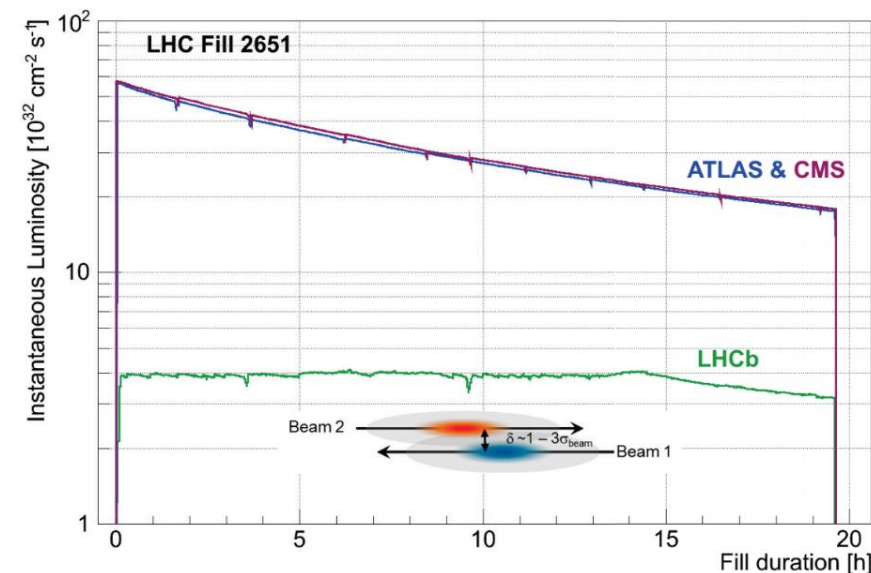
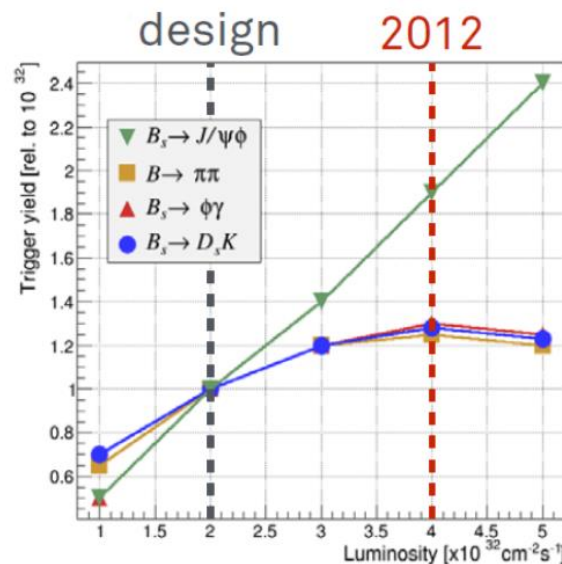
$$\mathcal{L} = 4 * 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$$

$$\mathcal{L} = 2 * 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$$

$$f = 1.1 \text{ MHz}$$

$$f = 40 \text{ MHz}$$

- Replacement of L0 hardware trigger with software trigger
- Adjustments in geometry, change in read-out electronics



Large Hadron Collider (LHC)

HL-LHC

