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Fully integrated digital readout for the new Fast Interaction Trigger for the ALICE upgrade

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ABSTRACT

Fully integrated digital readout, pulse analysis, extraction of time and charge, signal alignment, multiplicity analysis and trigger generation electronics were developed for the new **Fast Interaction Trigger (FIT)** as a part of the upgrade of the ALICE detector at the CERN LHC (Abelev et al., 2014 [1]; Trzaska, 2017 [2]). FIT will serve as the main luminometer, collision time, multiplicity, centrality, and reaction plane detector for the ALICE experiment during Run 3 and 4 of the LHC. Among the many challenges of this project are a high dynamic range (from 1 to 500 MIP per channel), requirement to operate with the sustained bunch crossing of 25 ns, provide single-MIP time resolution below 50 ps, complete the entire signal processing and trigger generation within 200 ns.

1. Introduction

FIT is made of two parts (Fig. 1) centered around the beam pipe and located on both sides of the interaction point (IP) [2]. FIT-A, shown on the left side of Fig. 1, is located 3.3 m from the IP. It consists of a large segmented plastic scintillator and an array of Cherenkov modules. The 1.48 m diameter scintillator disk is divided symmetrically into 45 degree octants.

The octants are subdivided into 5 rings of progressively increasing radii so that each ring covers equal presudo-rapidity range. Each outer sector connected to two PMTs to increase dynamic range and time resolution. In total there are 40 optically isolated sectors read out by 48 photosensors. The Cherenkov array of FITC, shown on the right side of Fig. 1, is curved to maintain constant distance (0.82 m) between the modules and the IP. For historical reasons, the scintillator ring is referred to as V0+ and the Cherenkov arrays, T0+. T0+ will use Planacon XP85002/FIT-Q — a modified MCP-PMT with a pore size of 25 μm [3] to detect light from fused silica radiators. To increase the granularity, the anodes of each sensor will be grouped into quadrants corresponding to 4 optically separated radiators coupled to the front window (Fig. 2) [4]. To reduce MCP aging and to obtain a sufficient dynamic range, a very low output amplitude of 10 mV/MIP at the MCP PMT output will be used. The signals will be sent over 34 m of double-shielded coaxial cables and processed by low-noise fast electronics. The intrinsic time resolution of the modified MCP-PMT is better than 13 ps. The signal attenuation on the cable if approximately 25%. To efficiently register the signals with 7.5 mV/MIP after cables system, FIT electronics must work with a 3 mV threshold corresponding to 0.4 MIP amplitude.

2. FIT DAQ Overview

The DAQ scheme of the FIT detector is shown in Fig. 3. The analog signals from the detector come to the Processing Modules (PM) were event time will be evaluated by a CFD and then digitized with 13 ps resolution. The input charge will be integrated and digitized by a 12 bits ADCs. Each processor module has 12 analog inputs, sufficient for the 3 T0+ modules. The digitized event data is sent to the Common Readout Unit (CRU) for storage and for further processing by the ALICE O2 system [5].

The data are transferred through 4.8 Gbps optical links using CERN proprietary protocol GBT [6]. This protocol includes Reed–Solomon error correction mechanism and has a well-defined data latency. The later allows transferring of the trigger information to the detector in the downlinks from the CRU. Also, all PMs send the digital “pre-trigger” data to the Trigger and Clock Modules (TCM V0+ and TCM T0+) via HDMI to process and generate the trigger. In total FIT electronics will be processing in parallel 256 (208 T0+ and 48 V0+) independent channels.

3. Front-end electronics

A 4-channel PM module prototype has been built and tested at INR RAS. It includes all the key components of the final PM but has a reduced number of input channels.

Fig. 4 depicts Front-End electronic (FEE) circuits. As the MCP-PMT signal rise-time is only 1.4 ns at the FEE input, the maximum CFD linear range is limited by the amplifier’s maximum output voltage slope. To

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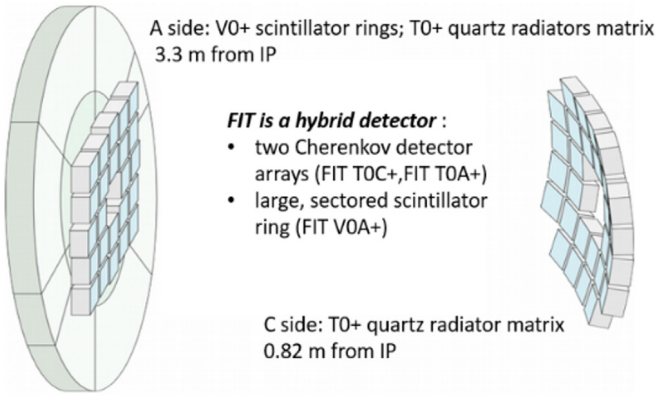


Fig. 1. Conceptual view of the two arms of the FIT detector.

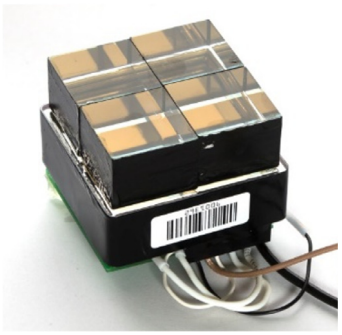


Fig. 2. MCP-PMT with coupled quartz radiator.

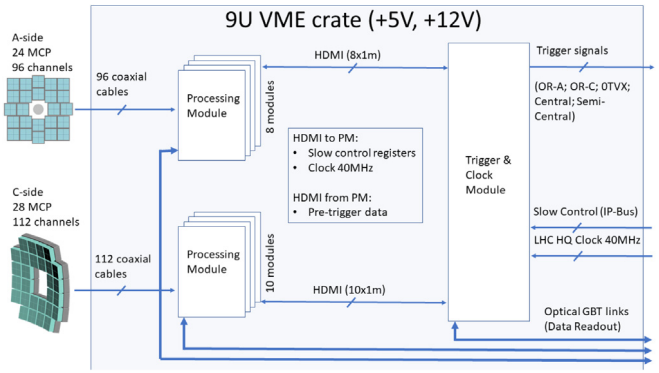


Fig. 3. FIT DAQ scheme.

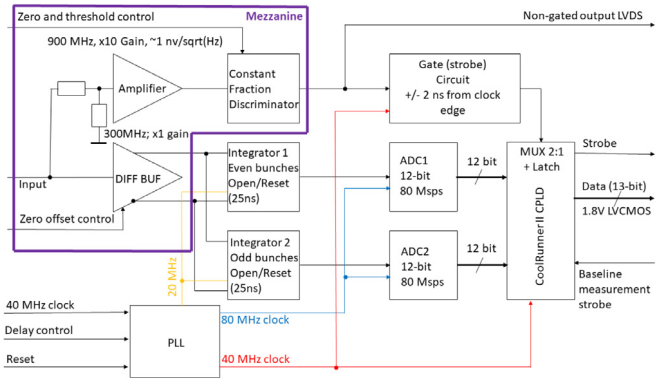
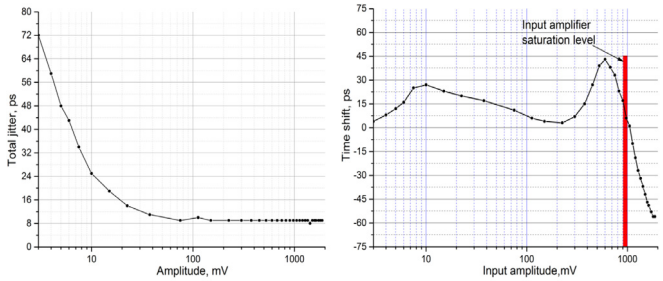


Fig. 4. Front-End Electronics for signals processing.



(a) Jitter vs. pulse amplitude. (b) "Time shift vs. pulse."

Fig. 5. FIT amplifier parameters.

get the maximum value for this parameter, the gain must be 10 or more. Consequently, the maximum input pulse amplitude for CFD is 300 mV (limited by the output saturation). The minimum value is 1 mV, limited by the thermal noise. As the signal threshold for FIT is 3 mV, we can simply decrease the input amplitude by a resistive divider, keeping CFD saturation at 900 mV. The channels with amplitude above 900 mV will be excluded from timing measurements for T0+. This however will not affect the precision of the detector, as in the case of high multiplicity events, only one non-saturated channel is sufficient to determine the interaction time.

The jitter dependence of the CFD timing from the input amplitude is shown in Fig. 5(a). The time shift–amplitude dependence is shown in Fig. 5(b). The MCP-PMT time resolution for the average pulse amplitude of 3 mV is 56 ps. The timing resolution for a 1 MIP pulse (7.5 mV averaged amplitude) is 27 ps.

The channels used for the charge measurement have their own input buffer, which allows to measure pulse charge with a higher dynamic range. There are two integrators and ADCs (Fig. 4) in each channel, while one integrates the signal, the other is in a reset state. The 25 ns reset time allows to measure signals at the threshold level just after the pulse with a maximal amplitude. The integrator has a "clean" integration window of at least 19 ns, which is sufficient to measure the signal charge without adjusting the phase of each ADC strobe. Strobe as the interaction signal timing is always within ± 2.5 ns from the central position. PLL allows fine adjustment of the integrator timing independently for each channel. The gating circuit checks whether has arrived in a correct time and sends the data strobe to the read-out electronics. The charge integrator input range is 0–2 V for T0+ part and 0–5 V for V0+. The 1 MIP pulse amplitude of 7.5 mV equals 15 ADC LSB for T0+ and 6 LSB for V0+. The noise level of the integrator is about 3 LSB, providing 1 MIP peaks resolution for the Cherenkov part of the FIT detector.

The timing information is digitized by the commercial 4-channel TDC THS788 (Texas Instruments). It has 4 independent channels with individual output interfaces. This TDC has high timing accuracy (8 ps RMS). The maximum processing delay (from input pulse to last bit sent) for the 8 bit TDC mode is 105 ns, for the 16 bit — 190 ns, with the same time resolution and extended time measurement range. LSB weight is 13 ps in any mode. If using 16 bit mode the processing delay will exceed the processing time limit for the FIT electronics. To decrease this time we use TDC in the 8 bit mode. This decreases the total timing data delay to 125 ns (from analog input to correct data in FPGA register), but makes the time measurements range insufficient. To correctly determine the time within the 25 ns period, we have build in PM FPGA TDCs with 400 ps resolution for each channel. The two LSBs of the "coarse" FPGA-based TDC and two MSBs of the "fine" external TDC overlap.

The weight of overlapped MSB is 833 ps. The time shift between FPGA-based and external TDC do not exceeds 200 ps. This makes possible to merge correctly the information from both TDCs. After comparison of overlapped bits, the result MSBs (measured in FPGA) are

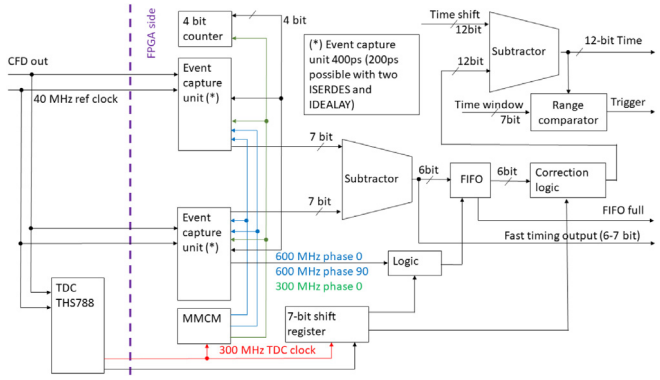


Fig. 6. Low delay TDC based on THS788 and FPGA.

increased or decreased by 1 if overlapped bits do not coincide. Fig. 6 demonstrate clocks distribution and data flow of common TDC module. To capture the input signals with the needed precision, four-phase 600 MHz FPGA clock is required. This clock is formed from the 300 MHz readout clock of the THS788 TDC.

4. Online trigger processing

LM (Level -1) is the fastest trigger required by ALICE. The upper limit for LM trigger processing by FIT electronics is 225 ns. The LM trigger data processing will be done in the two-level FPGA processor, based on the Kintex-7 Xilinx FPGAs with a 320 MHz main clock. The trigger and Clock Module (TCM) receives the amplitude and time data from all PM modules in the system (up to 20). For vertex and multiplicity triggers two identical systems of the two-level pipelined adders are used, but for vertex trigger the time is normalized in TCM on number of the active channels per side to calculate average time, for multiplicity trigger the total sum per side is used for trigger decision.

Each PM sends to TCM the sum of amplitudes and times as well as the number of active channels in the event. TCM compares the total charge sums with the two predefined threshold values and, accordingly, generates two multiplicity triggers (Central and Semi-Central). If at least one channel on each side of the detector comes within the preset interaction time range, TCM forms ORA an ORC trigger. ORA/ORC triggers means registered at least one charge particle at A/C sides in correct interaction time that is used for the optimal trigger to start physics with pp collision. If the difference between the average times from each side is within the predefined thresholds, TCM forms Vertex (TVX) trigger signal indicating that the longitudinal position of the IP is within the required range interval. These signals are sent to the ALICE Central Trigger Processor (CTP) [7]. The measured trigger delay is 203.5 ns, which is slightly less than the calculated 208 ns assumed for the worst timing conditions. The TCM also provides commands and configuration through the 1 Gb Ethernet optical link via IP-BUS protocol and transmits important parameters, such as event counters to the Detector Control System. The TCM also provides synchronous high-quality clock for all PMs.

5. Conclusions

The project has already satisfied the requirements and passed the Engineering Design Review. Prototypes of both PM and TCM have been built and tested and the 205 ns total processing trigger time was confirmed. The first prototypes of the sensor and the front-end electronics have been installed inside of the ALICE magnet and were used to collect the data from LHC collisions since 2016.

Acknowledgments

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