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Front end electronics and first results of the ALICE V0 detector

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ABSTRACT

This paper gives a detailed description of the acquisition and trigger electronics especially designed for the V0 detector of ALICE at LHC. A short presentation of the detector itself is given before the description of the Front End Electronics (FEE) system, which is completely embedded within the LHC environment as far as acquisition (DAQ), trigger (CTP), and detector control (DCS) are concerned. It is able to detect on-line coincident events and to achieve charge (with a precision of 0.6 pC) and time measurements (with a precision of 100 ps). It deploys quite a simple architecture. It is however totally programmable and fully non-standard in discriminating events coming from Beam–Beam interaction and Beam-Gas background. Finally, raw data collected from the first LHC colliding beams illustrate the performance of the system.

1. V0 detector

1.1. Functions of the detector

The V0 detector [1] is a small angle detector consisting of two arrays of 32 scintillating counters, called V0A and V0C, which are installed on either side of the ALICE [2] interaction point of the two LHC beams. This detector has several functions. It provides Minimum Bias triggers and Centrality Triggers for the central barrel detectors in pp and A–A collisions. It measures the charge of the particles and the time of their arrival in each of the 64 channels.

In practice and during normal operation, both arrays are required (AND mode) to provide triggers, namely: Minimum Bias trigger (MB), Multiplicity Trigger (MT), semi-Central Trigger (CT1) and Central Trigger (CT2). Since interactions of beam particles with the residual gas of the vacuum chamber generate tracks through the ALICE sub-detectors, the V0 detector is able to provide Minimum Bias p-Gas triggers (PG). An OR mode can also be adopted. In that case, the absence of Minimum Bias Trigger from V0C alone can sign trigger due to p-Gas background events through the ALICE muon spectrometer.

In pp collisions, the efficiency of V0 for detecting at least one charged particle in both sides is about 84% when backgrounds from the hardware environment are introduced. Finally, the V0 detector participates in the measurement of luminosity with a precision as good as 10%. Detailed studies can be found in [3].

1.2. Detector layout

The V0A is located 330 cm away from the vertex on the side opposite to the muon spectrometer. The V0C is fixed at the front face of the hadronic absorber, 90 cm from the vertex. They cover

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the pseudo-rapidity ranges $2.8 < \eta < 5.1$ (V0A) and $-3{:}7 < \eta < -1{:}7$ (V0C) for collision vertex at the central position. They are segmented into counters distributed in four rings (Table 1).

Table 1
V0A and V0C arrays. Pseudo-rapidity and angular acceptances (deg.) of the rings.

Ring	V0A		V0C	
	η_{max}/η_{min}	$\theta_{min}/\theta_{max}$	η_{min}/η_{max}	$\theta_{max}/\theta_{min}$
0	5.1/4.5	0.7/1.3	−3.7/−3.2	177.0/175.3
1	4.5/3.9	1.3/2.3	−3.2/−2.7	175.3/172.4
2	3.9/3.4	2.3/3.8	−2.7/−2.2	172.4/167.5
3	3.4/2.8	3.8/6.9	−2.2/−1.7	167.5/159.8

Extensive tests were performed to choose the best design for the individual counters and the easiest integration of the disks in the system. The material consists in BC404 [4] scintillating material (2.5 and 2.0 cm in thickness for V0A and V0C, respectively) with 1 mm in diameter BCF9929A Wave-Length Shifting (WLS) fibres [4]. The V0A array is constructed with the fibres spaced by 1 cm and embedded in the two transverse faces of the segments following the “megatile” technique. There are 32 individual counters arranged in 4 rings and 8 sectors of 45°. The V0C array has the fibres grouped by layers of 9 units and glued along the two radial edges of the segments. There are 48 individual counters of this type distributed following two inner rings of 8 counters and two outer rings of 16 counters. The latter are connected 2×2 to make a single detection element. A picture of each array is shown in Fig. 1.

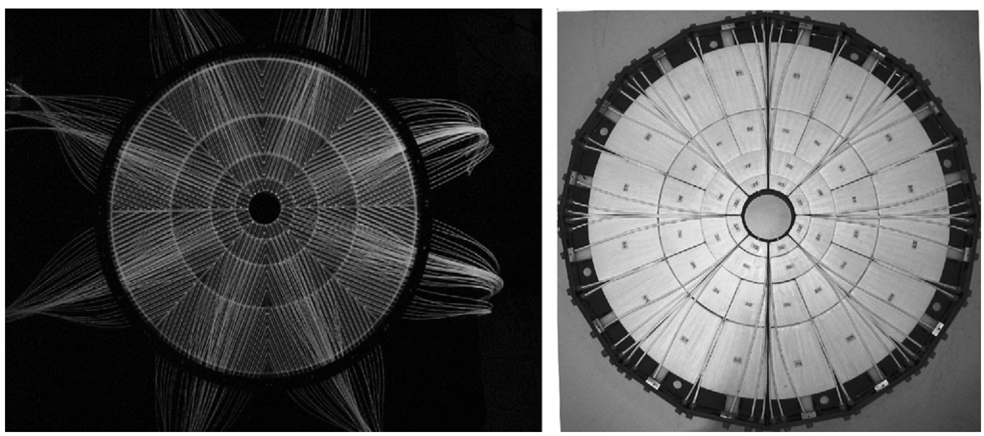

Fig. 1. Front pictures of the V0A (left) and V0C (right) hodoscopes before casing.

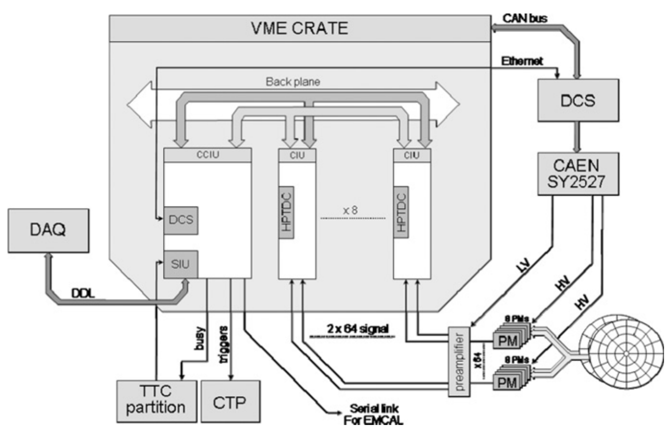

Fig. 2. Block diagram of the V0 Front End Electronic.

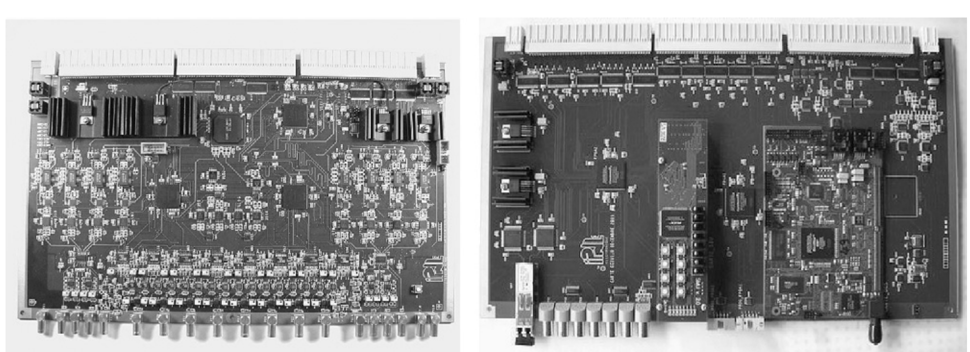

Fig. 3. Pictures of the CIU (left) and CCIU (right) boards of the V0 Front End Electronics.

Photomultipliers (PMT) R5946 (hybrid assemblies H6153-70) from Hamamatsu [5] collect the light. They are fixed on the V0A disk holder in groups of 4 units and connected directly to the WLS fibres. They are installed on the absorber in groups of 8 units for the V0C and connected to counters through Mitsubishi [6] optical fibres 3.22 m long.

The signal provided by each PMT is sent to an electronics circuit, which delivers two signals. The first one is sent to a threshold discriminator for the generation of the V0 triggers. It is amplified by a factor of about 10 and clamped at the level of 300 mV. The second one, not amplified, is used for the measurement of the charge given by the counter. The two treatments are carried out far from PMTs, namely 25 m away.

2. Electronic description

The Front End Electronic provides signals for triggering the ALICE experiment at the level L0 and digitizes the physical signals delivered by the individual scintillating counters. The system generates four trigger types and several sets of information listed hereafter (cf. Block diagram Fig. 2).

2.1. Triggers

- *A minimum bias trigger*: This trigger is generated if the number of channels fired during a collision is at least 1 on V0C and 1 on V0A. The detection of the fired channels is made by means of 2 observation windows (Section 3), one for V0A (named BBA) and the other one for V0C (named BBC).
- *Two beam-gas triggers*: One for the beam-gas coming from the V0A side of the ALICE detector, the other one for the beam-gas coming from the V0C side. The detection of the beam-gas is done by the use of two specific observation windows, BGA and BGC, in partnership, with respectively, BBC and BBA (Section 3).

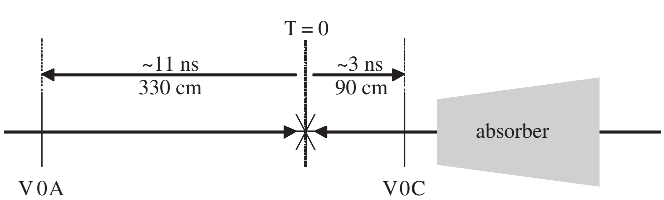

Fig. 4. Time of flight of particles issued from a collision at the vertex to the V0A and V0C disks.

- *A centrality trigger of the collision*: This trigger is generated if one or the other, or both following conditions are fulfilled:
  1. The number of channels fired during a collision is larger than a programmed trigger generation. This signal is based on observation windows (Section 3).
  2. The integration charge seen during a collision is larger than a programmed trigger generation threshold. This signal is based on a charge integrator (Section 4).
- *The multiplicity of Minimum Ionizing Particles* (*MIPs*): This measurement is obtained in two different ways
  1. the anode charge digitization based on charge integrator (Section 4),
  2. the pulse length measurement proportional to the charge of the pulse (Section 5).

2.2. Other information

- The time difference between the detected particles and the beam crossing signal (BC) (Section 5).
- The V0 electronics of both array systems (V0A and V0C) is located in one VME crate. This 11U VME crate is used for its mechanical structure, which can accept 9U modules and for its supply voltage. There is no VME controller in the rack. All boards plugged on the VME back plane are full customs. They do not use the VME bus but a specific back plane. Two types of boards are plugged in the crate
- *The CIU board* (*Channel Interface Unit*): It performs charge and time digitization of 8 channels. 8 boards of this type are necessary for the acquisition of the 64 channels (Fig. 3(left)).
- *The CCIU board* (*Channel Concentrator Interface Unit*): It performs the collection of the data from the 8 CIU boards and provides interfaces with the external world for the acquisition (DAQ), slow control (DCS), clock (BC) and trigger systems (CTP) (Fig. 3(right)).
- The used FPGA are from the ALTERA cyclone family (EP1C12F325C6), the configuration program is written in VHDL and stored in an EPCS4 EEPROM, which is loaded at power up. There are 3 FPGA of this type per CIU board and two for the CCIU board.

3. Flag detection structure

The V0 has to detect and segregate on-line the Beam–Beam from the Beam-Gas collisions. It is thus necessary to verify on each disk (V0A and V0C) and for each clock period (25 ns), the event occurrence at the expected times, namely 11 ns after the collision on V0A and 3 ns after the collision on V0C for Beam–Beam interaction, (Fig. 4), 11 ns before the bunch crossing time on V0A disk for Beam-Gas coming

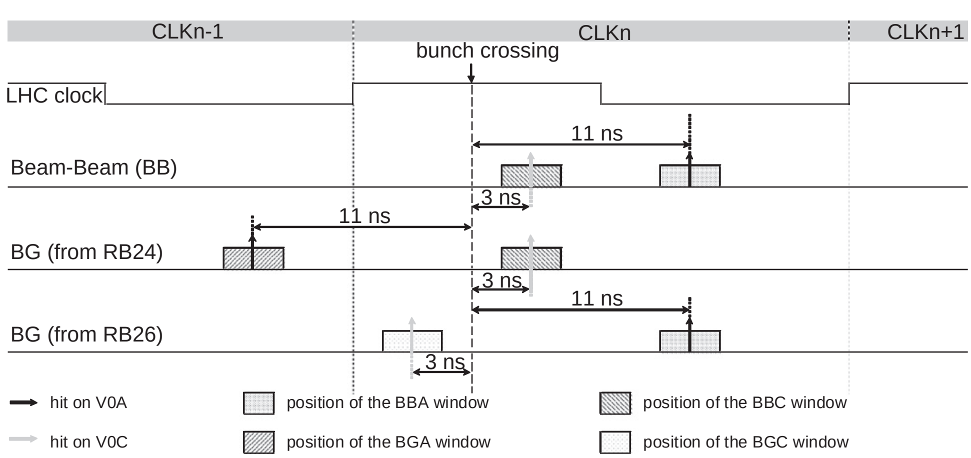

Fig. 5. Time alignment diagram for BB, BGA and BGC type events.

from the V0A side, and 3 ns before the bunch crossing time on V0C disk for Beam-Gas coming from the V0C side (Fig. 5).

The detection of the hit on each channel is achieved using several observation windows. A BBA flag corresponds to a hit coming inside the BBA window (and similarly for the others flag). The electronic systems allowing this detection is built around a simple D flip flop circuit. The hit signal is connected to the clock input. The D input is connected to a window signal, which is active around the time when the hit is supposed to come. The result of the detection is available on the Q output and collected by a FPGA, which also performs the reset and the latch of the flip flop.

A priori, the phase of the hit relatively to the LHC clock is not known. It is thus necessary to have a device allowing the adjustment of a time window anywhere inside the 25 ns interval between two consecutive LHC clocks. The reset and the latch signals of the flip flop have to be attached to the time window too. All these signals are established through configuration in a FPGA module. A 5 bit shift register is used at a frequency 5 times faster than the 40 MHz of the LHC clock (Fig. 6). At the reset signal time, the configuration of the signal profile is loaded in the shift register. When active (release reset), the register configuration is propagated from stage to stage at the frequency of 200 MHz. The output of the last register is thus a signal of 25 ns period, which can be configured by step of 5 ns according to the chosen profile.

In order to have a time window adjustable with a precision of 10 ps, an additional device is used and connected to the previous one. It is based on the use of two shift registers, providing two different window profiles. These two signals are then delayed by a value ranging from 0 to 5 ns thanks to the MC10EP195 component (resolution of 10 ps). Finally, a logical AND between the two signals is achieved, resulting in the required window (Figs. 7 and 8).

The whole device described above allows to setup the beginning and the end of the time windows with a precision of 10 ps, and to collect and analyse the results obtained by each window, whatever the position within the period of the LHC clock is. Moreover, their widths cannot exceed 10 ns so that the FPGA circuit can provide latch and reset of the flip flop.

The data thus collected are used on-line to create a group of triggers called Minimum Bias, Beam-Gas from V0A side and Beam-Gas from V0C side. These triggers are L0 level triggers for the full ALICE experiment, namely all ALICE sub-detectors. They are also stored then sent to the acquisition system for off-line analysis. In order to facilitate the research of the event-clock (n) correlation, all data in the time range $[n-10, n+10]$ are sent to the DAQ. It is then very easy to detect pile-up, misalignment of data, etc (Fig. 11).

4. Charge integrator structure

The V0 Front End Electronics is able to measure on-line the charges delivered by the 64 photomultipliers. Their integration is achieved at each clock period, namely every 25 ns. In order to have

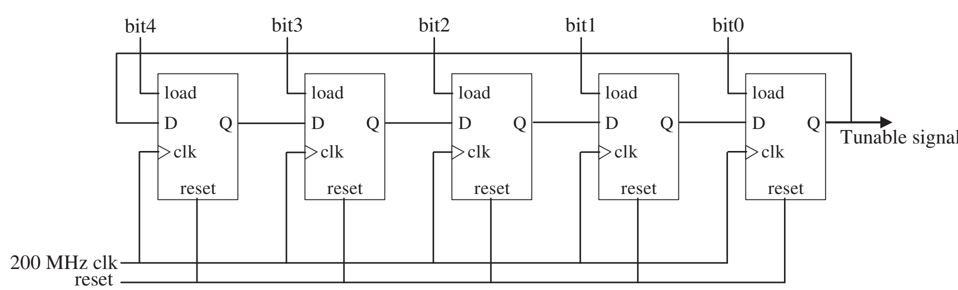

Fig. 6. Shift register for the window profile generation.

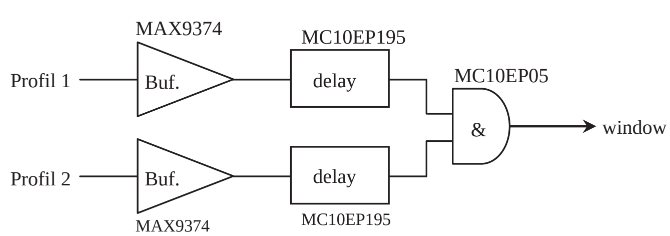

Fig. 7. Final stage for the generation of the observation window.

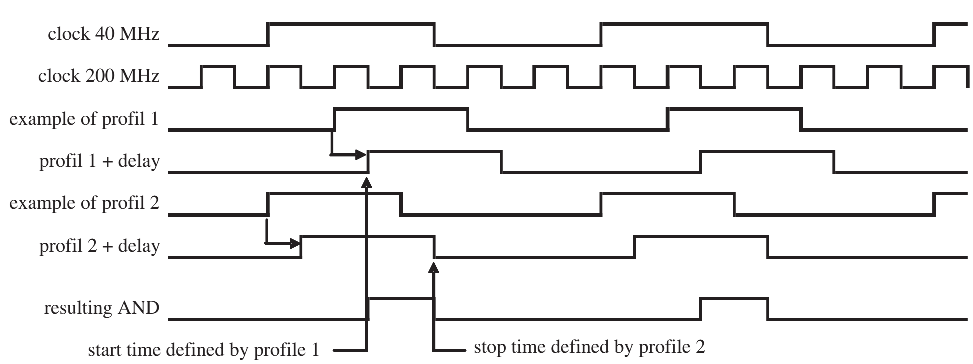

Fig. 8. Timing diagram.

no dead time, two integrators are used, working alternatively. During the integration by one circuit, the other one executes its reset, then vice versa. The times for the integration, the reset and the digitalization of the signal are fully programmable through slow control. A sketch of the double integrator system is shown in Fig. 9.

The signals which pilot the reset of the integrator and the digitalization through analog to digital conversion (ADC) of the charge are delivered by a FPGA circuit which uses the technique of the shift register with loading of their profiles. However, contrary to what is done for the time windows, a complete integration cycle is provided during two consecutive clock periods. The shift register of this function is thus made of 10 flip flop circuits instead of 5 at the frequency of 200 MHz. The frequency of the obtained signal is 20 MHz. It defines for each integrator and in 50 ns the two sequences of integration, namely (1) the integration phase, (2) the reset. This device leads to generate command signals programmable by steps of 5 ns. It is thus easy to set the beginning and the end of the integration gate with steps of 5 ns. The total width can thus be adjusted from 5 ns to 35 ns maximum (Fig. 10).

The collected charge data are used on-line to create two supplementary triggers called Centrality and Semi-Centrality. These triggers are used as L0 level triggers for the full ALICE experiment. These charge data are also stored then sent to the acquisition system for off-line analysis. In order to ease the off-line treatment of events correlated to a clock period n, all data in the time range $[n-10, n+10]$ are sent to the DAQ.

5. Timing measurement structure

In order to identify off-line with an optimum precision the Beam–Beam and Beam-Gas events (Fig. 5), the electronics measures the time of arrival of particles on V0A and V0C channels with a resolution of 100 ps (HPTDC feature). Moreover, a second charge measurement is done from the measurement of the pulse width with a resolution of 400 ps (HPTDC feature). These two time values are sent to the acquisition system for an off-line analysis.

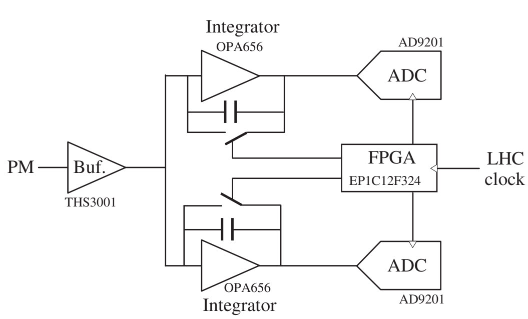

Fig. 9. Dual high speed integrator block diagram.

The main component of this function is the HPTDC [7], a High Performance Time to Digital Converter developed in the microelectronics group at CERN. There is one HPTDC module per CIU board. It provides these time measurements for the 8 channels of one V0 ring.

6. First results in pp collisions at LHC

First proton–proton collisions of the CERN Large Hadron Collider (LHC) occurred in November 23, 2009. Obviously, the V0 detector was a part of the ALICE apparatus collecting data used for physics measurements [8]. Moreover, these first proton–proton collisions provided the best conditions for fine final adjustment of the electronic system. This section gives results obtained at this time using the Front End Electronics described above.

Fig. 11 gives the distribution of the flags provided by the 64 channels of the V0 detector. The data correspond to a few Beam–Beam events signed by flags aligned on the LHC clock 0 of the bi-dimensional distribution (Section 3). The flags appearing at LHC clocks $[-1, -10]$ of the distribution are due to noisy channels providing "after-pulses". If such an effect is present simultaneously in the V0A and V0C sides and aligned on the same LHC clock, an "after-trigger" will be produced. This background trigger effect is due to the very low collected light and consequently to the high voltage applied to photomultipliers. Several solutions are being analysed to minimize this effect.

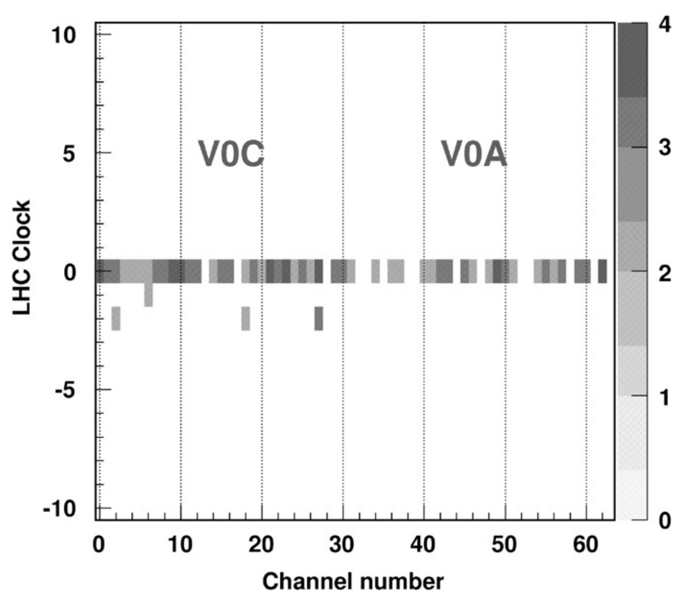

Fig. 11. Distribution of flags from proton–proton events provided by first LHC collisions in 2009 (Section 3). Here the width of the time windows is 25 ns.

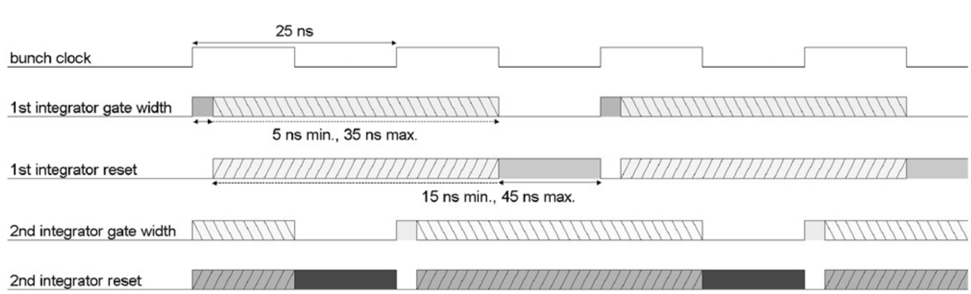

Fig. 10. Dual high speed integrator system timing.

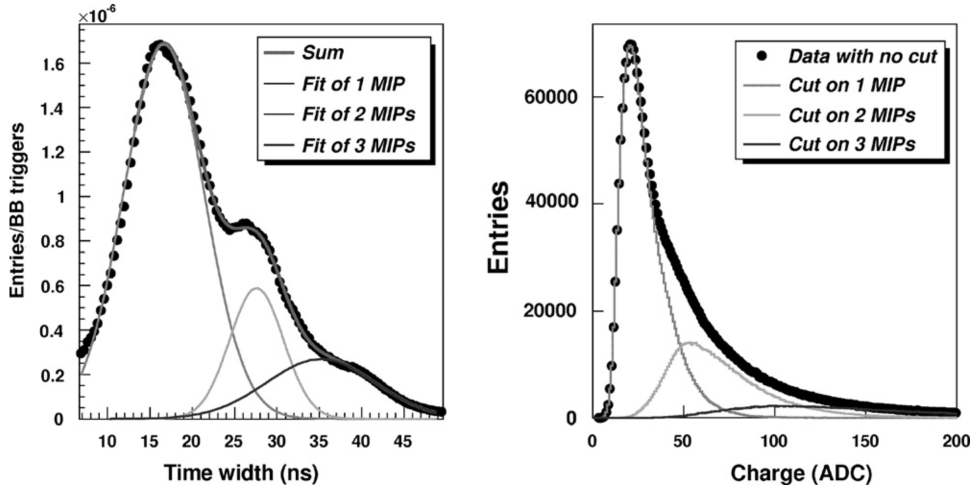

Fig. 12. Distributions of the photomultiplier signal widths (left) provided by HPTDC circuit (section 5) and charges (right) provided by integrator circuits (Section 4) from the V0A channels.

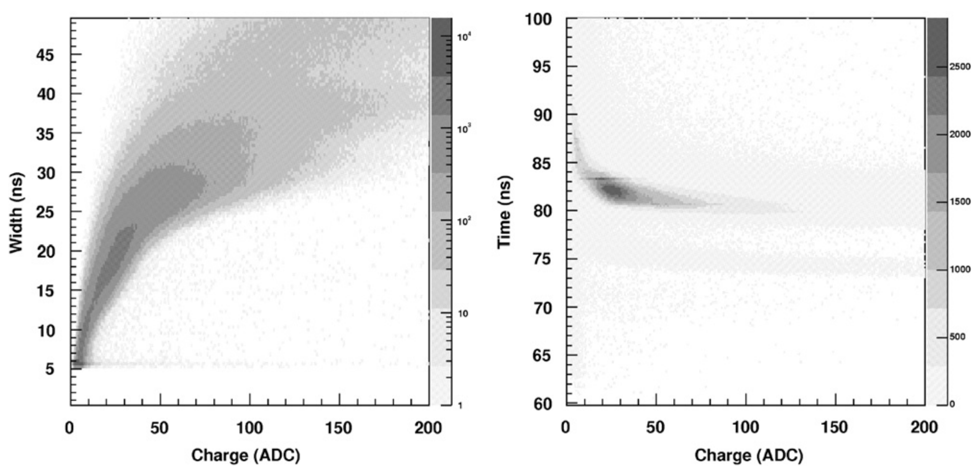

Fig. 13. Correlation between the integrated charge of the photomultiplier signals with the signal width (left) and the leading time (right) from the V0C channels.

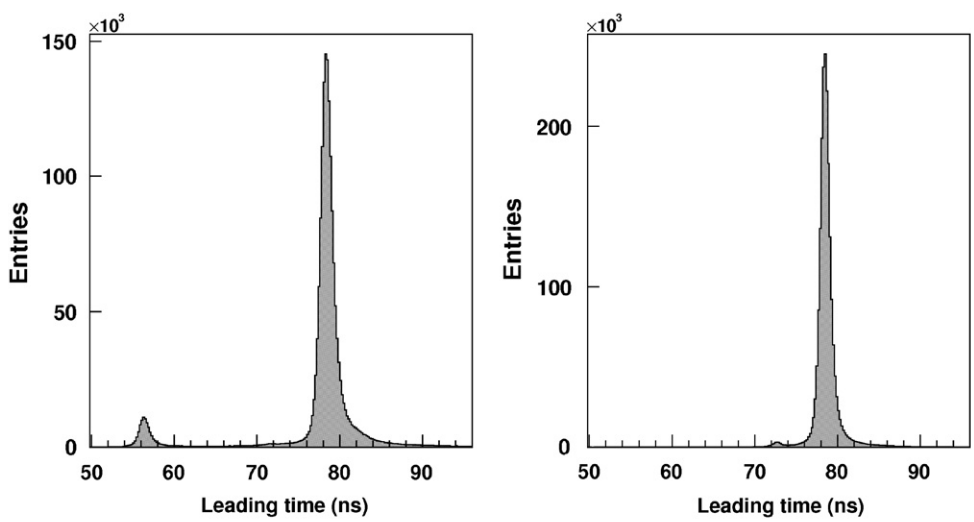

Fig. 14. Time distribution of particles arriving on the V0A disk (left) and V0C disk (right) relatively to the crossing time of the two LHC beams (Section 5).

Fig. 12(left) gives the width distribution of the 32 signals coming from the V0A photomultipliers. This distribution clearly shows a three bump structure revealing the presence of one, two and three MIPs as simulated by Gaussian functions. The corresponding charge distribution plotted in Fig. 12(right) does not reveal such a structure, showing a low light signal provided by each individual

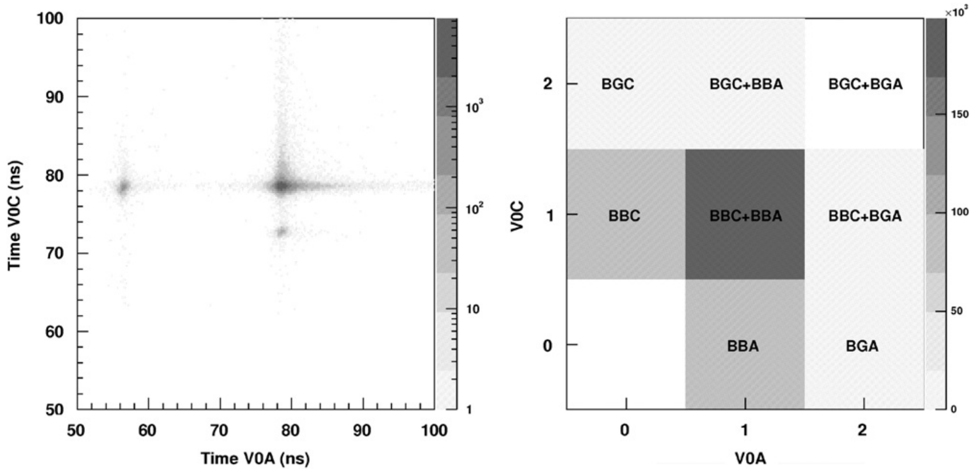

Fig. 15. Correlation between the arrival time of particles in the V0A and V0C disks (left). Each store of events corresponds to a specific type of trigger provided by the V0 detector (See Section 3 and Fig. 5 for explanations). Yield of individual classes of events (right) together with the corresponding trigger label (See Section 3 and Fig. 5 for explanations). The zone around [0,0] corresponds to external triggers with no track through both V0 disks.

detector. Nevertheless, by selecting events within a window around the MIP in Fig. 12(left), the charge corresponding to the MIP value can be isolated (Fig. 12(right)), providing the calibration of the individual channels. The correlation of the two previous parameters recorded from the V0C disk is shown in Fig. 13(left).

Fig. 14 gives the leading time distributions of the 32 V0A and 32 V0C channels. The largest peaks contain all Beam–Beam events and Beam-Gas events from the C side (Fig. 14(left)) and from the A side (Fig. 14(right)). The smallest peaks contain only Beam-Gas events from the A side (Fig. 14(left)) and from the C side (Fig. 14(right)). The time difference between peaks corresponds to -22 ns and -6 ns, respectively, (Fig. 4), namely twice the time of flight of particles between the collision point and the corresponding V0 disk. A two-dimensional representation of these parameters is shown in Fig. 15(left). Finally, the time given by V0C channels is shown in Fig. 13(right) as a function of the integrated charge. The threshold discrimination reveals a dependence of the time with the signal amplitude. After a correction offline to minimize this effect, a resolution of the order of 700 ps is obtained. Nine types of events with their statistics can be extracted, depending on the existence and/or the value of the measured time. Their name, given in Fig. 15(right) has a straightforward meaning (Section 3).

7. Conclusion

This paper describes the Front End Electronics of the ALICE V0 detector and gives the raw results obtained from the first collisions provided by LHC at 900 GeV in 2009.

The widths of the observation windows for the generation of the triggers were set to their maximum value during these tests, namely 25 ns. Their efficiencies for shorter widths have not been measured because the procedure for their alignments required beam time not available at this period.

The use of a double integrator system appeared to be very well adapted to the readout of PMT signals at the frequency of 40 MHz, providing no dead time. The first tests on collisions showed a charge resolution of 0.6 pC per channel with a sharing of 95% of the charge in the period of the beam crossing and 5% in the following one.

The measure of the time by HPTDC appeared to be very precise and useful. It allows to determine the leading edge of the PMT signals for the separation of Beam–Beam events from Beam-Gas events in the one hand, to measure their width providing the multiplicity of the detected MIPs when their number is a few of units, in the other hand.

In conclusion, the Front End Electronics system of the V0 detector was fully functional but not perfectly adjusted during the first collisions of protons beams at LHC when 284 pp events were recorded. It worked perfectly and allowed the first data analysis and physics results [8].

Before the next data recording, an optimisation in situ of the setup for the adjustment of the relative calibration of all the 64 channels (high voltage values) and the precise adjustment of the integration gates and time windows (widths and positions) will be carried out. The ultimate performance of the system can thus be quantitatively evaluated.

Acknowledgments

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