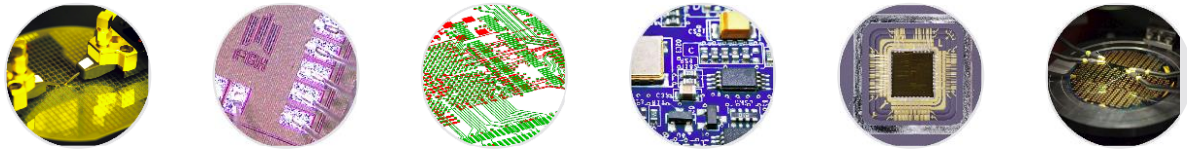
Microelectronics Group
Dept. Measurement and Electronics
AGH University of Science and Technology

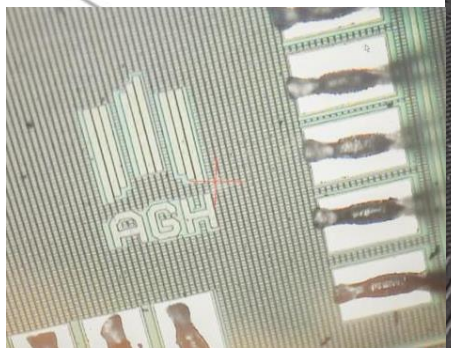
Radiation Imaging Systems

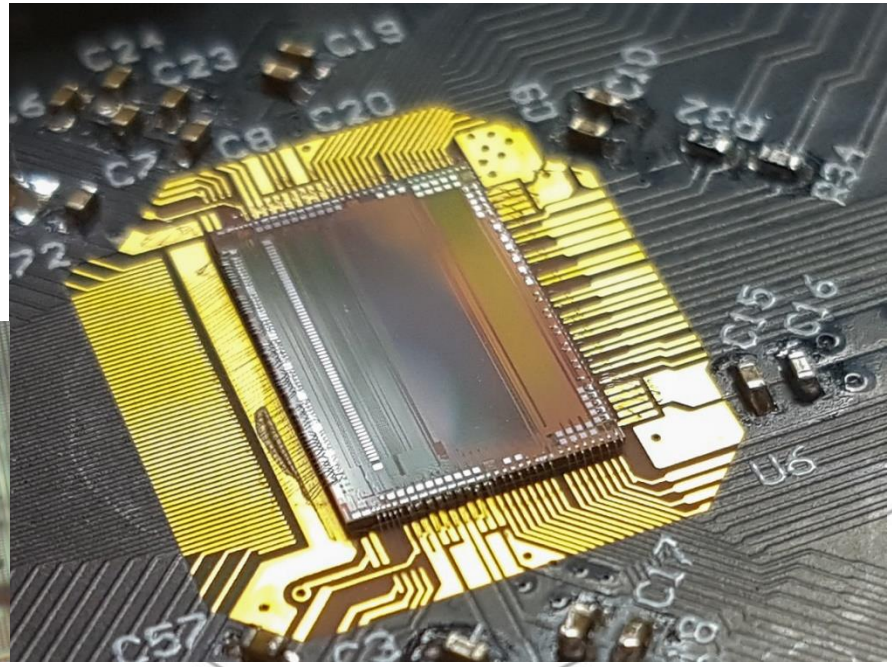


dr inż. Krzysztof KASIŃSKI, dr hab inż. Piotr Maj
kasinski@agh.edu.pl

AKADEMIA GÓRNICZO-HUTNICZA IM. STANISŁAWA STASZICA W KRAKOWIE
AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

AGH





Our expertise and experience

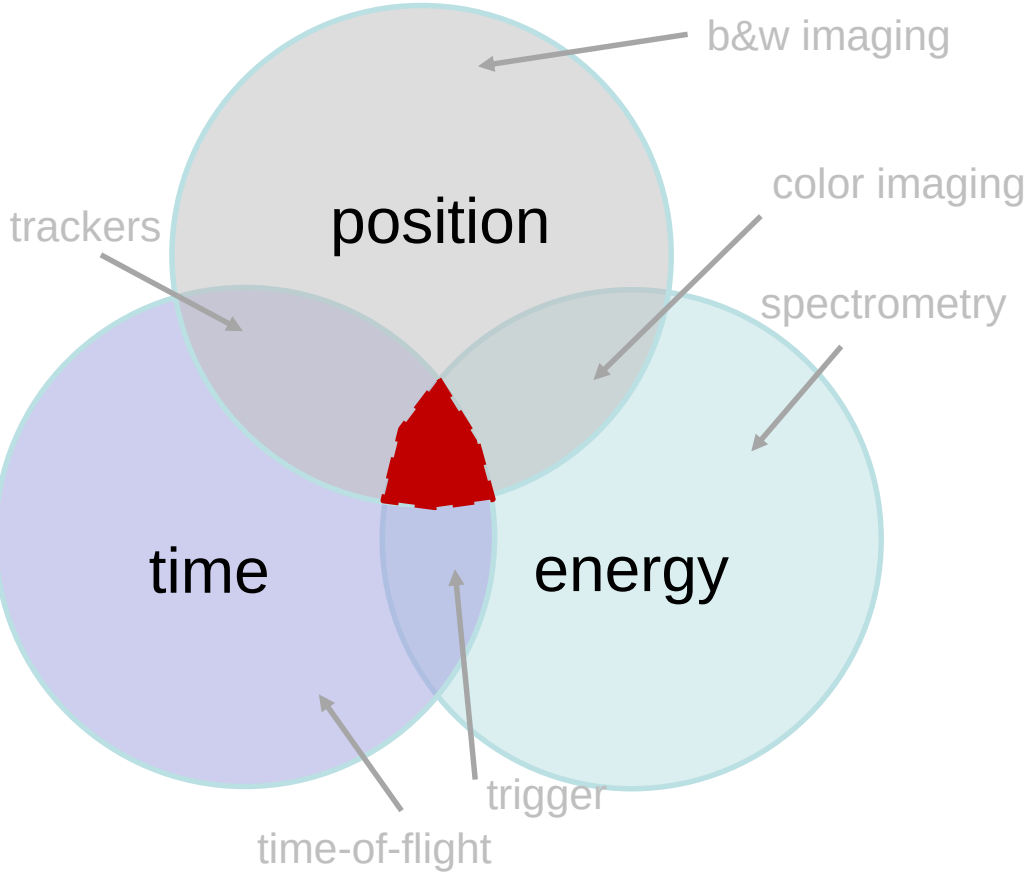
mixed signal (analog and digital) circuits design

Multichannel, integrated circuits design for radiation imaging

- hybrid pixel detectors, single-photon counting
  - photon counting (energy window)
  - ultra-high speed charge processing & frame-rate
  - low noise and high parameter uniformity
  - charge sharing compensation

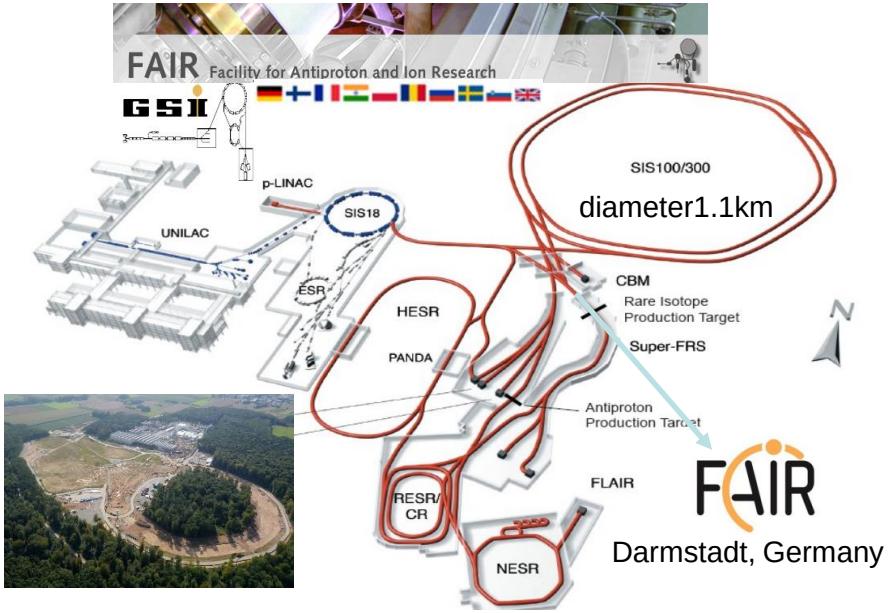
- readout circuits for Si microstrip & GEM detectors
  - time and amplitude measurement (ADC in-channel)
  - radiation hardening techniques

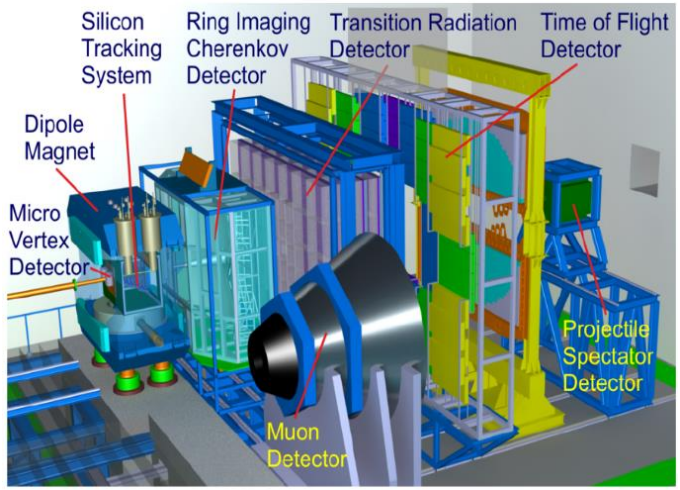
- < 40 nm CMOS up to 180 nm CMOS technologies



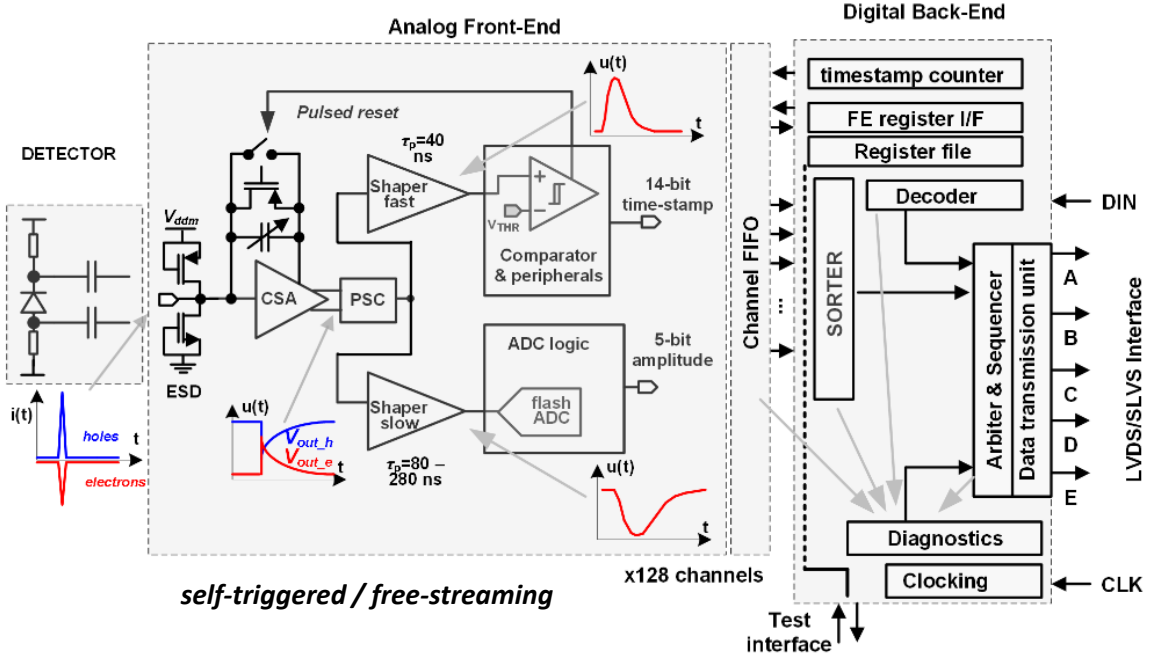
Amplitude & Time Measurement IC for Silicon Microstrip and GEM detectors at CBM

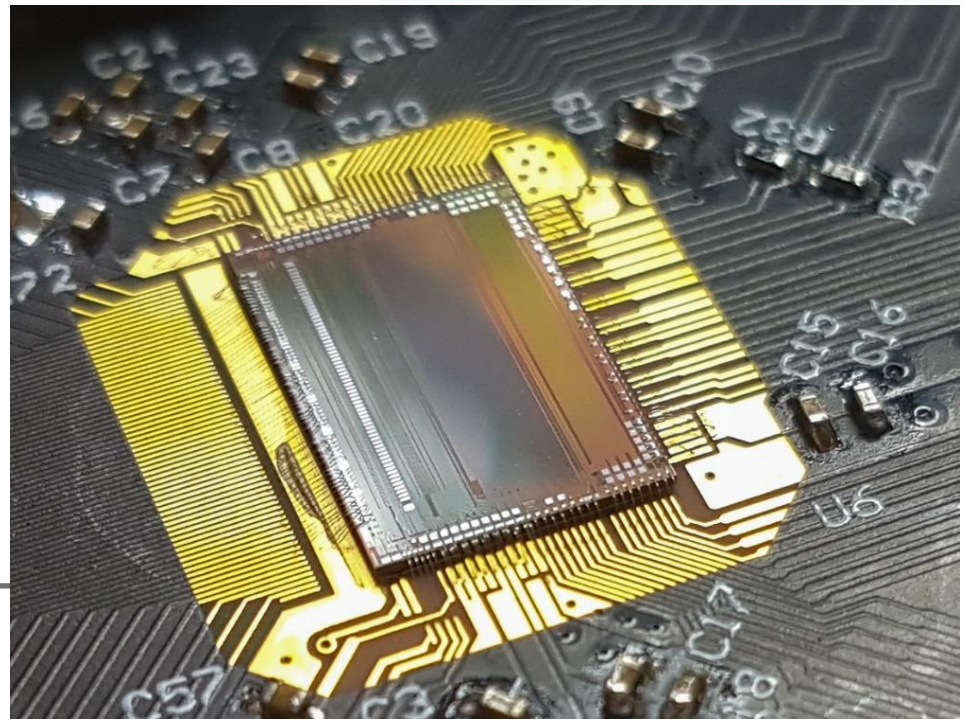
AGH



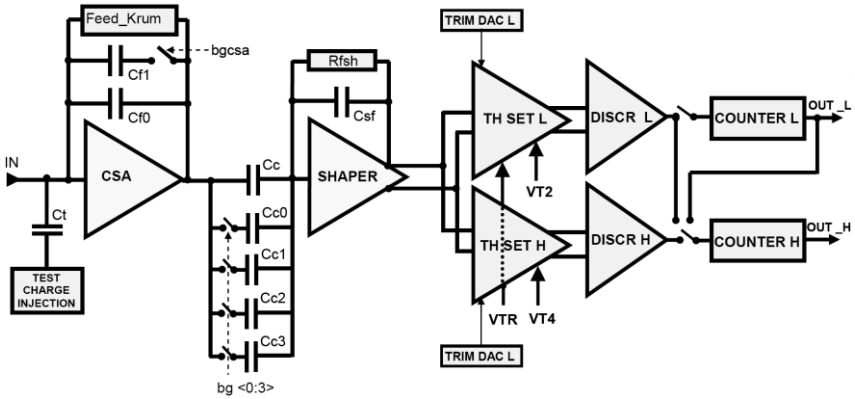


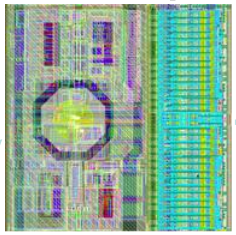
Parameter	Value
Names	STS/MUCH-XYTER2 / SMX2
Process	180 nm CMOS MM/RF
Chip area	10.0 mm × 6.75 mm
Channel number	128 + 2 test
ADC bits	5
Input charge frequency	max. 500 kHz
Power Consumption:	
Uninitialized	0.6 – 1.2 W/chip
Initialized	1.023 W/chip @ I_d=2 mA 8 mW/channel
Offset spread of fast channel	1.12 mV rms / 0.015 fC rms (after correction)
Offset spread of ADC [fC]	0.09 (before correction) [39] 0.02 (after correction)
Gain	
Fast shaper (STS)	73 mV/fC
Slow shaper (STS)	32.7 mV/fC
Gain spread:	
Fast shaper	0.8 %
Slow shaper	0.5 % (after calibration)
ENC (Equivalent Noise Charge)	
Fast shaper	44 e^-/pF + 583 e^- rms
Slow shaper	27 e^-/pF + 538 e^- rms
Slow shaper peaking time [ns]	90 / 180 / 262 / 332



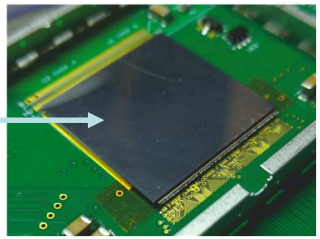


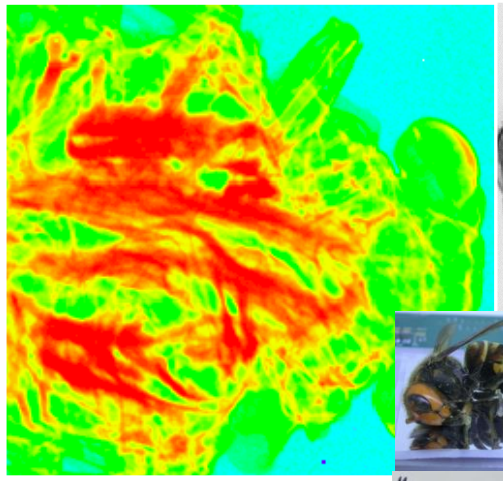
Ultra-Fast X-Ray Imaging Chip for Synchrotron Applications (32 k pixels)

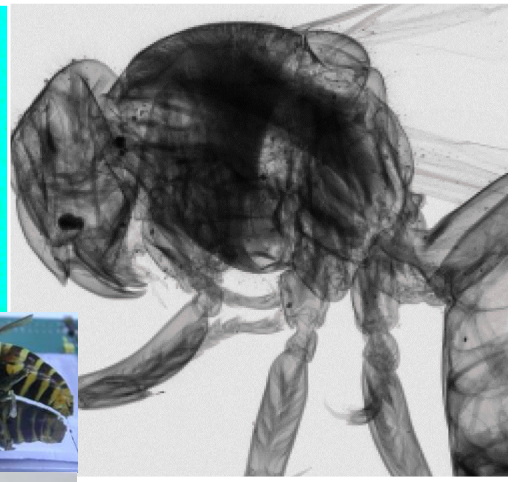


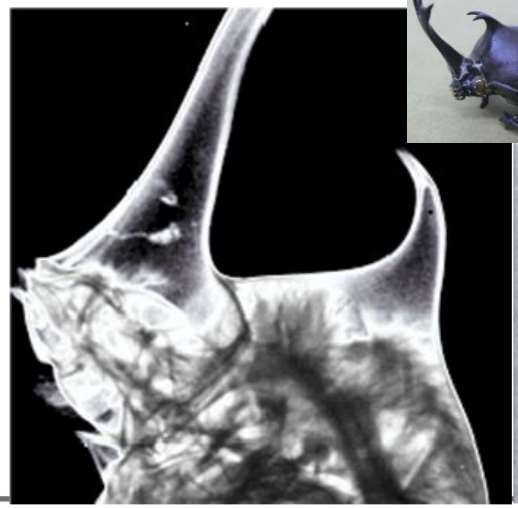


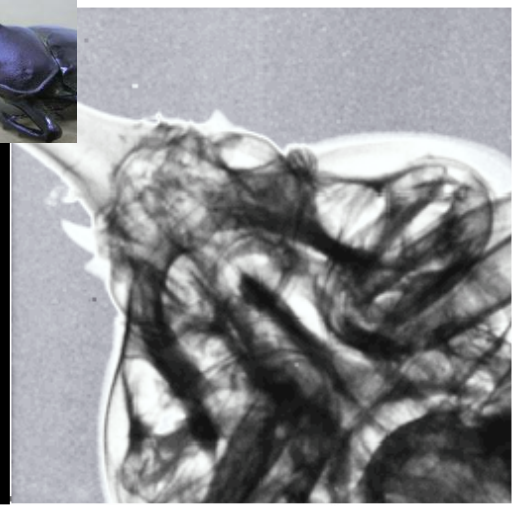
75 x 75 μm^2 pixel











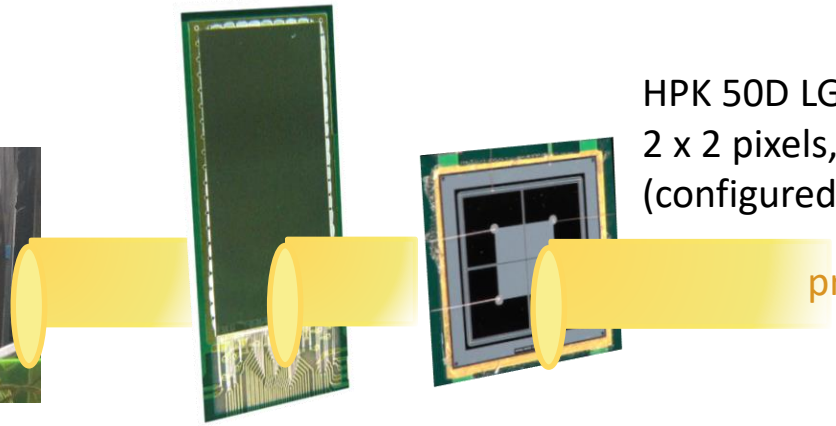
Camera prototype:

- Built with two UFXC32k IC
- 65536 pixels
- > ~100 Millions of Transistors
- Low noise: 120 electrons rms.
- High data throughput: 3.2 Gbit/s/chip.
- more than 50 000 fps
- Energy-window mode,
- High dynamic range mode,
- Zero dead-time mode
- 3-sides buttable module
- USB, ETH, Camera Link Interfaces

Testing setup

Fermilab

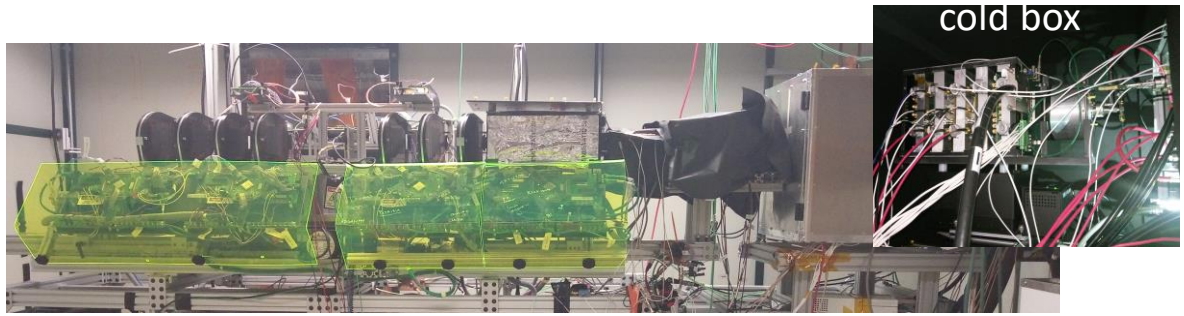
Tracker: FTBF telescope 7 planes of strips
each 60 µm pitch, 15 deg

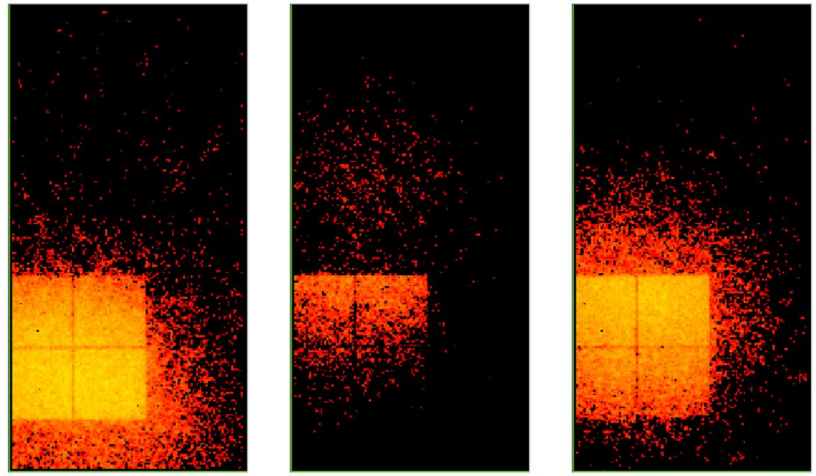


HPK 50D LGAD
2 x 2 pixels, 3 mm pitch each
(configured ~1 000 triggers/spill)

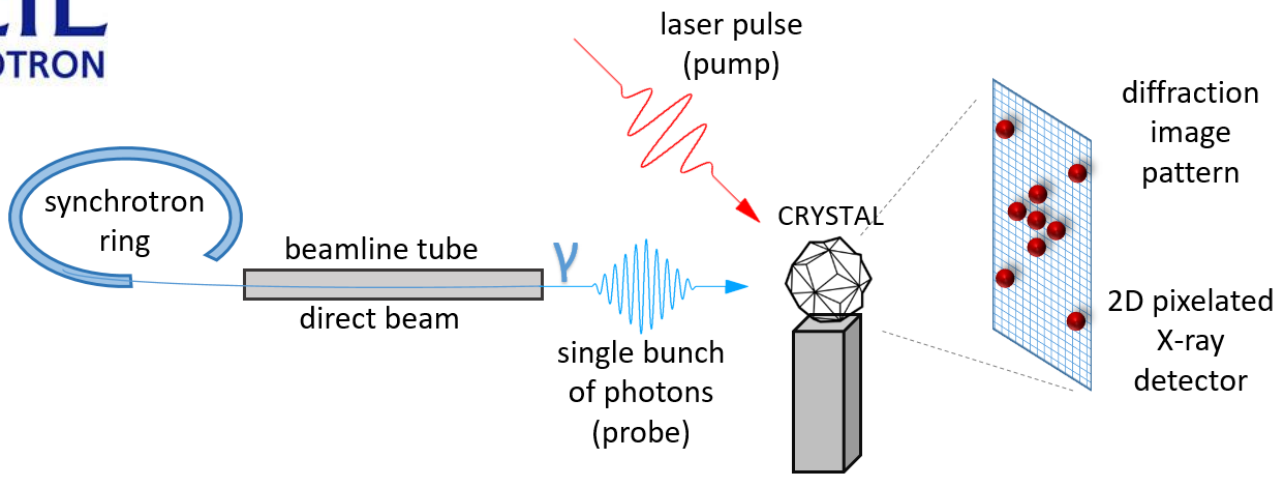
protons

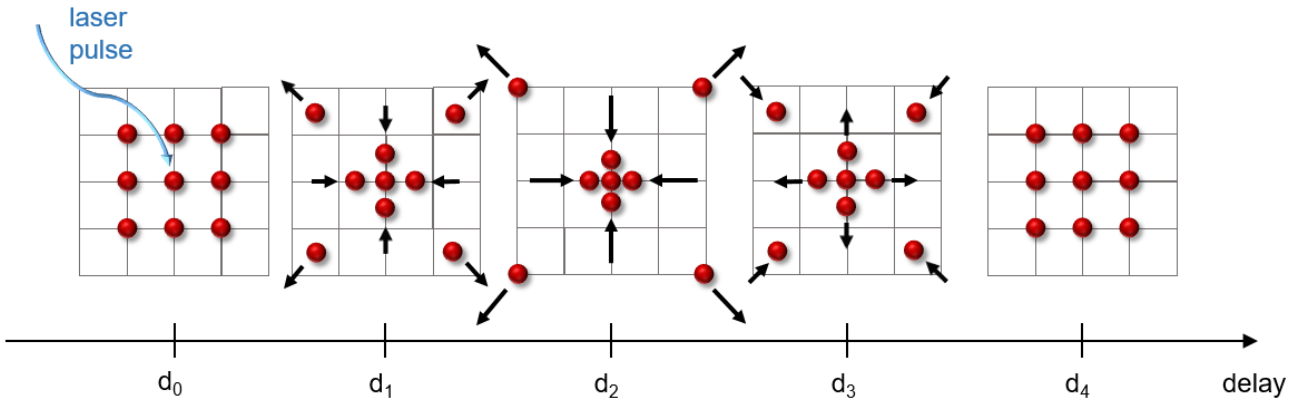
UFXC32k SPC HPAD,128 x 256 pixels,
75 µm pitch each 320 µm silicon sensor





Tests for pump-probe experiment in SOLEIL

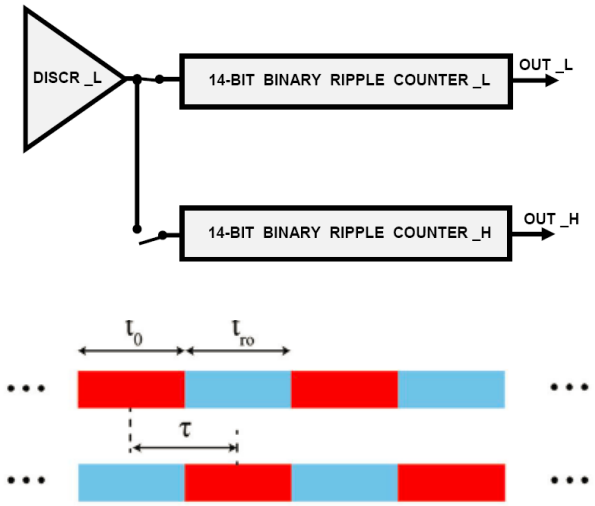


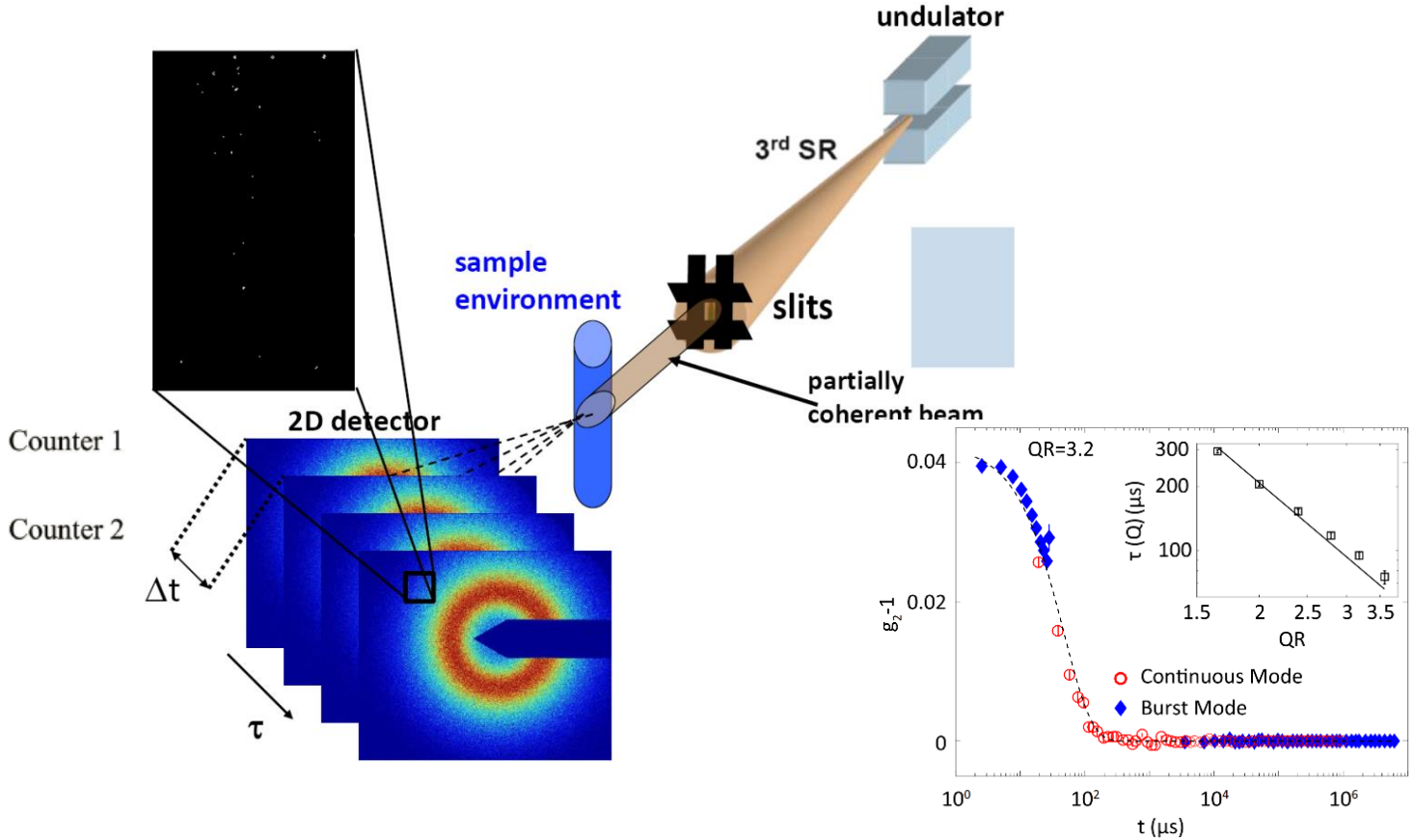


X-ray Photon Correlation Spectroscopy
at Advanced Photon Source in ANL

Argonne NATIONAL LABORATORY

Unique technique to probe the motion of nanoscale structures over a wide range of length (100 nm – 1 nm) and time scales (10^{-6} – 10^{3} seconds) in materials

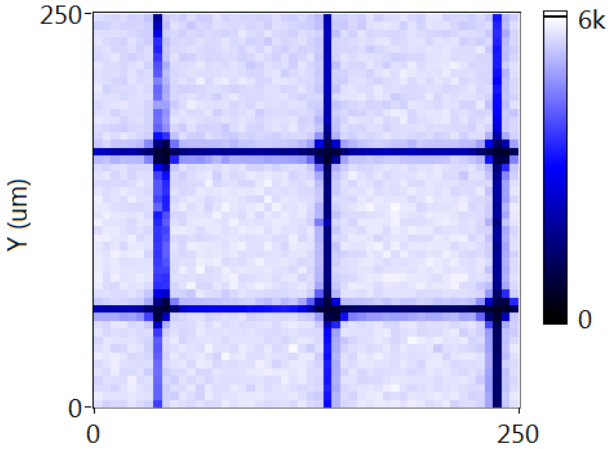


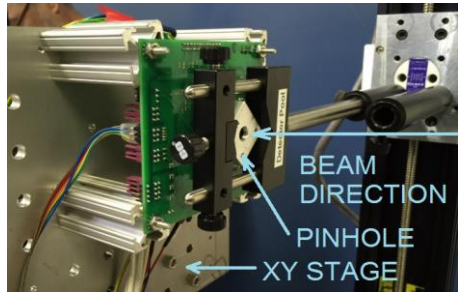


XY scaning with step 5 um (pencil beam ϕ= 3.5um) - ANL

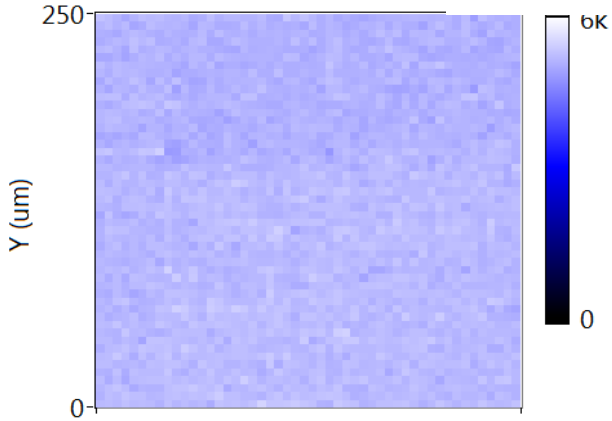
Argonne NATIONAL LABORATORY

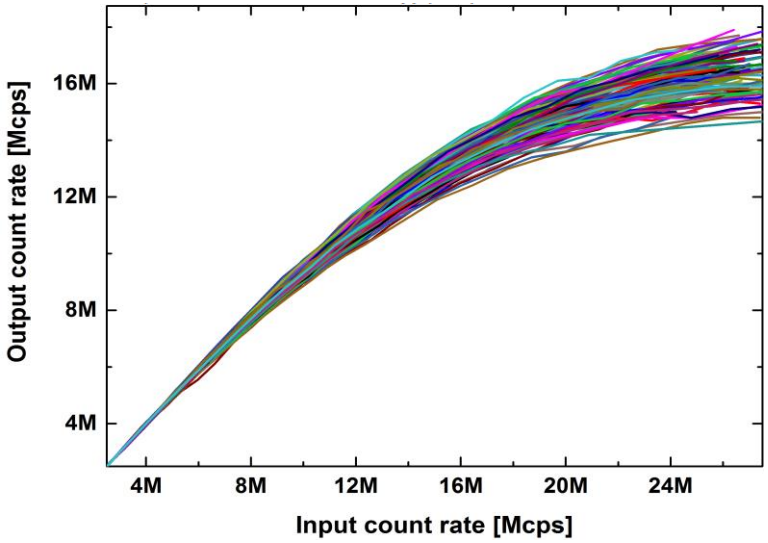
Standard counting





C8P1





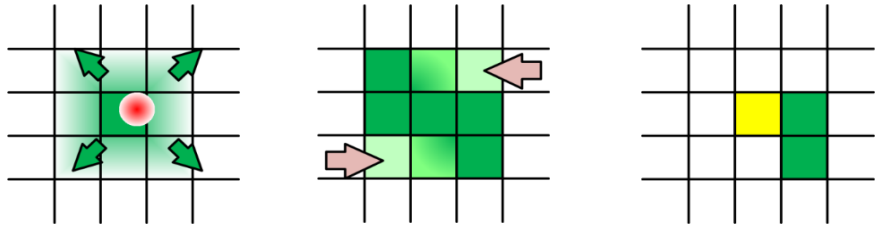
Mode	This work	
	FAST_HC	FAST
Process	40 nm	
Pixel size [μm^2]	100×100	
Power/pix. [μW]	103	46
ENC [e^- rms]	185	212
10% dead time loss input rate # [cps/pixel]	12 M	12 M
10% dead time loss input rate # [photons mm^{-2} s^{-1}]	1.2 G	1.2 G

for count ratio N_{OUT}/N_{IN} = 0.9

Pixel Readout with Asynchronous Approximation of a Center of Gravity of a Charge Distribution from a Radiation Conversion Event

Argonne NATIONAL LABORATORY

New approach based on pattern recognition. Allocate a hit to a single pixel basing only on the form the area affected by the charge cloud



Formation phase ⇒ Contraction phase ⇒ Resolution phase

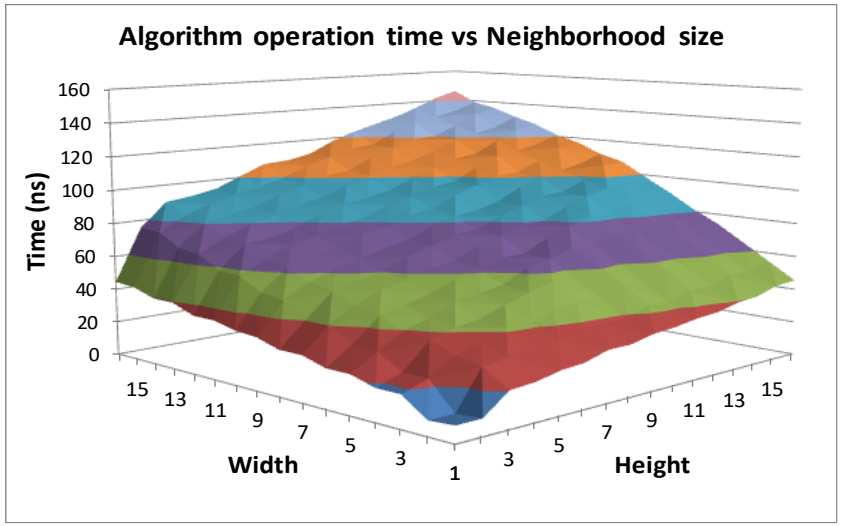
Advantages:

- Limited analog processing circuitry (shaper/amplifier, summing node, discriminator).
- Shorter hit processing time.

Challenges:

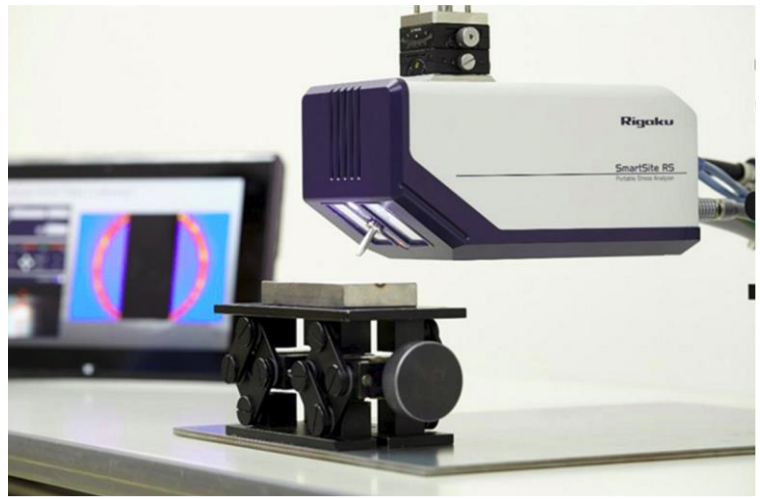
- Dealing with asynchronous nature of the events
- Identification of pixels belonging to the same event.
- Hit allocation algorithm.

Tested prototype in GF 55nm
(digital part only)



P.Otfinowski, G. Deptuch, P. Maj
IEEE JSSC 2017

Pixel & Microstrip ASICs for Diffractometry in Commercial Applications



D/teX Ultra, a one-dimensional imaging device which increases the precision of measurement while shortening measurement time.

Hypix 3000, a two-dimensional, 16-chip X-ray pixel camera based on the PXD18k ASICs. It belongs to the fastest cameras of this type in the world, and additionally, it is capable of recording photons of precisely determined energy and can operate in a zero dead-time mode.

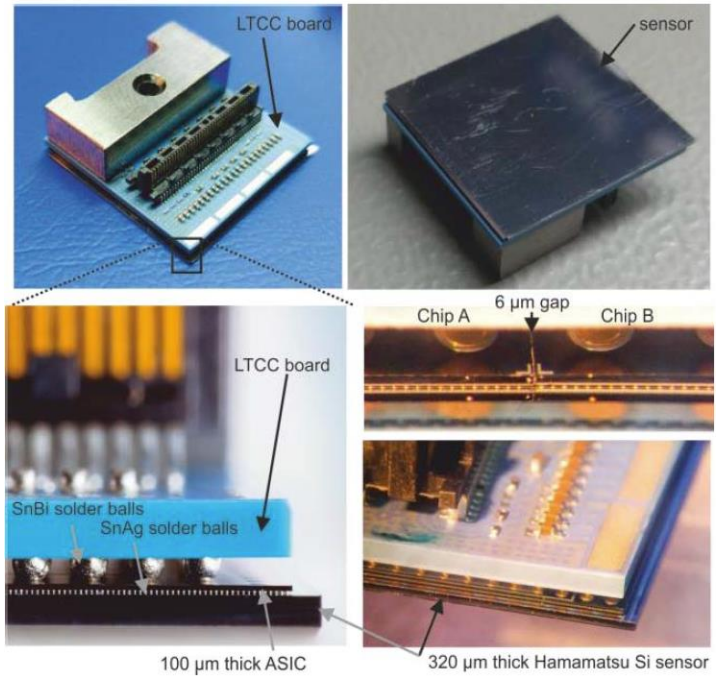
SmartSite RS, one of the world's smallest portable analysers of stress in metals (up to 200 mm of inner diameter). It uses a the observation of "Debye-Scherrer diffraction rings" of a thin beam of X-rays reflected from the tested element.

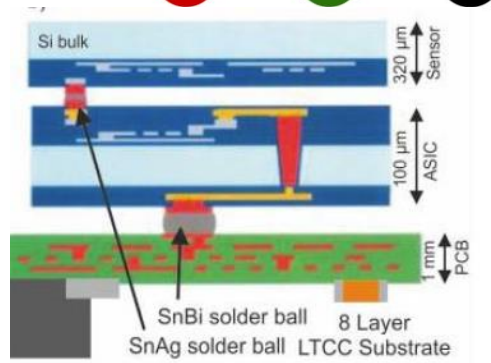
Rigaku
Leading With Innovation

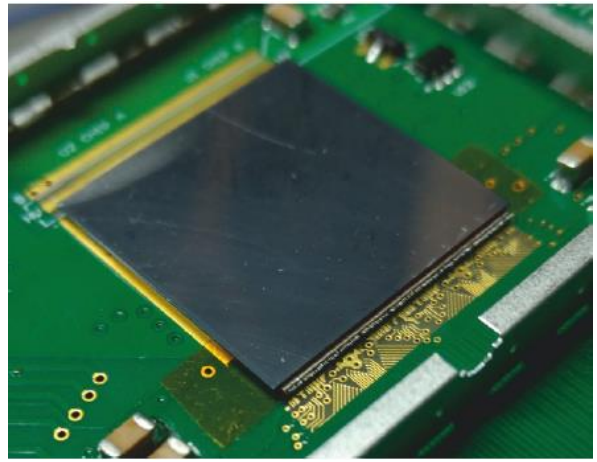
Our expertise and experience

Radiation imaging microsystems design

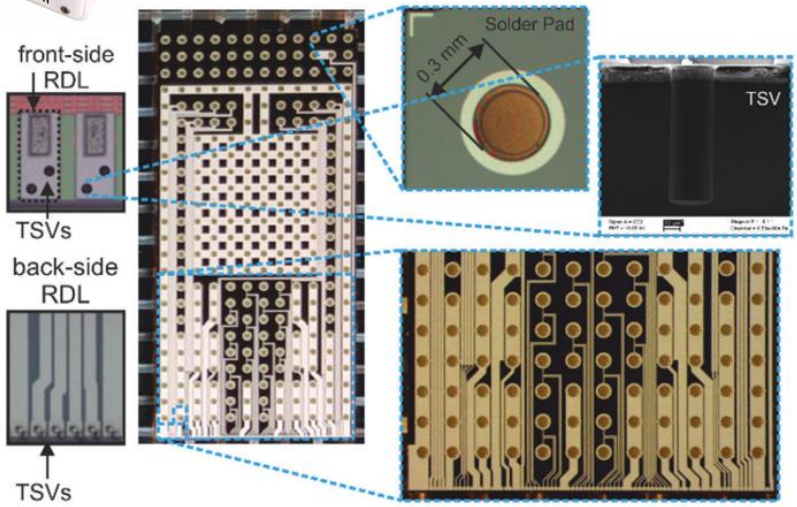
- Advanced 3D Microintegration Techniques
  - through-silicon via
  - redistribution layer, flip-chip







- **Printed Circuit Boards design**
  - mixed-signal: ultra low noise analog & high-speed digital
  - signal integrity, power integrity, thermal analyses
  - FR4 & ceramic substrates, wire-bonding (in-house)
  - wafer probe cards, digital cameras, etc.
- **Software Design**
  - FPGA-based readout (NI PXIe Hardware)
  - Automated test software (NI LabVIEW)
  - Microcontroller-based systems design



Cooperation and Network

X-ray Imaging Hybrid Pixel Detectors

- Fermi National Laboratory, USA
- Argonne National Laboratory, USA
- Synchrotron SOLEIL, France
- Rigaku Corporation, Japan
- KEK, Spring8, Japan
- Fraunhofer IZM Institute for Reliability and Microintegration, Germany
- University College, Ireland
- IMEC, Belgium

Integrated Circuits for HEP Trackers

- GSI Helmholtzzentrum Fuer Schwerionenforschung, Germany
- FAIR Center, Germany
- WUT, Warsaw
- Variable-Energy Cyclotron, Kolkata, India
- CBM Collaboration (55 countries)
- CERN
- IMEC, Belgium

Cadence Academic Network
National Instruments Center of Excellence
Europractice (Cadence & Mentor)

IEEE Solid-State Circuits Society Chapter Poland

- yearly ~5 events, inviting most renowned industrial & academia experts in various fields of microelectonics
- Organization of 2019 45th ESSCIRC/ 49th ESSDERC Cracow, Poland (AGH, WUT, UJ, CEZAMAT)

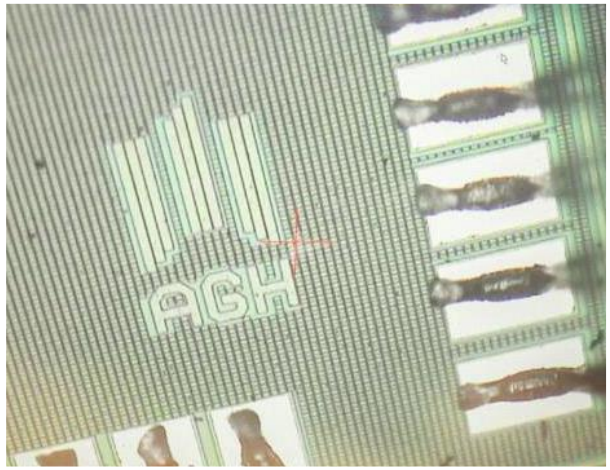
Numbers

Microelectronics group

More than 270 scientific papers / patents / books since 2006

More than 55 Integrated Circuits Designs fabricated and tested

More than 24 Research Grants / Industry Projects since 2007



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dr hab. inż. Grzegorz Deptuch
dr hab. inż. Marek Miśkowicz, prof. n.
dr hab. inż. Piotr Maj, prof. n.
dr hab. inż. Mirosław Żołądź, prof. n.
dr hab. inż. Piotr Kmon, prof. n.
dr inż. Krzysztof Kasiński
dr inż. Rafał Kłeczek
dr inż. Piotr Otfinowski
dr inż. Aleksandra Krzyżanowska
mgr inż. Anna Kozioł
mgr inż. Weronika Zubrzycka
mgr inż. Łukasz Kadłubowski
mgr inż. Piotr Kaczmarczyk

More at:
http://www.kmet.agh.edu.pl/katedra-metrologii/zespoly-badawcze/asics/