The development of the readout ASIC for the pair-monitor with SOI technology ~irradiation test~

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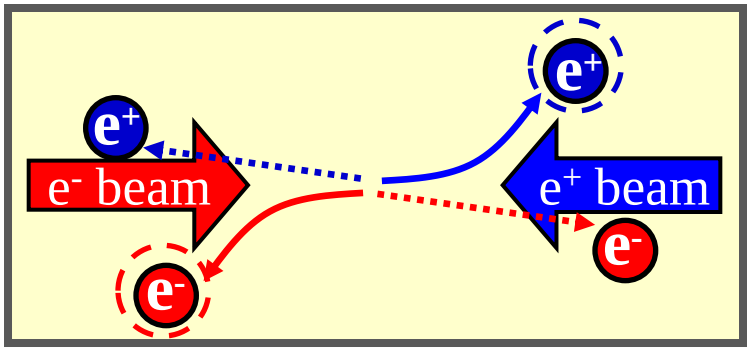
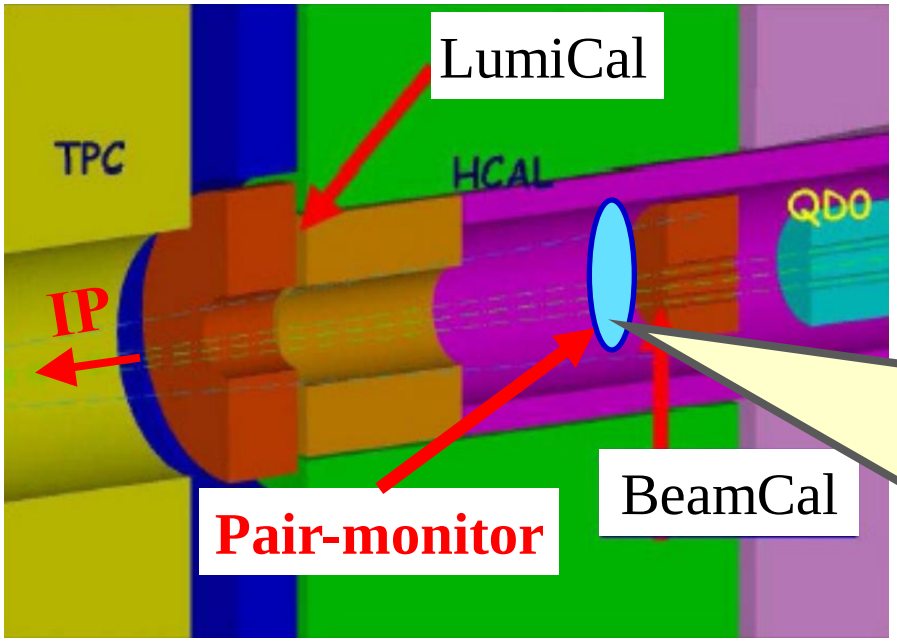
- Introduction
  - Pair-monitor
  - SOI technology
- Prototype ASIC
  - Design
  - Irradiation test

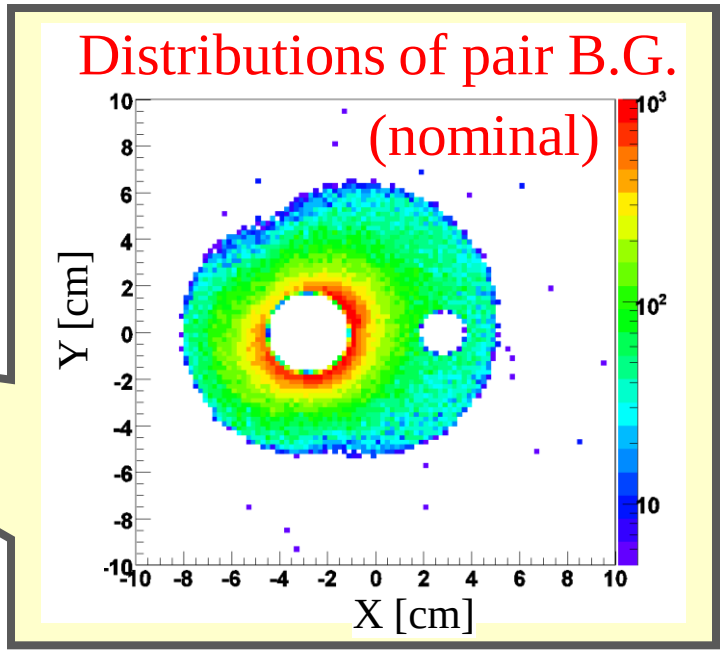
Pair-monitor

Pair-monitor is a silicon pixel detector to measure the beam profile at IP.



- The distribution of the pair B.G. is used.
  - The same charges with respect to the oncoming beam are scattered with large angle.
  - The scattered particles have information on beam shape.
- The location will be in front of the BeamCal.



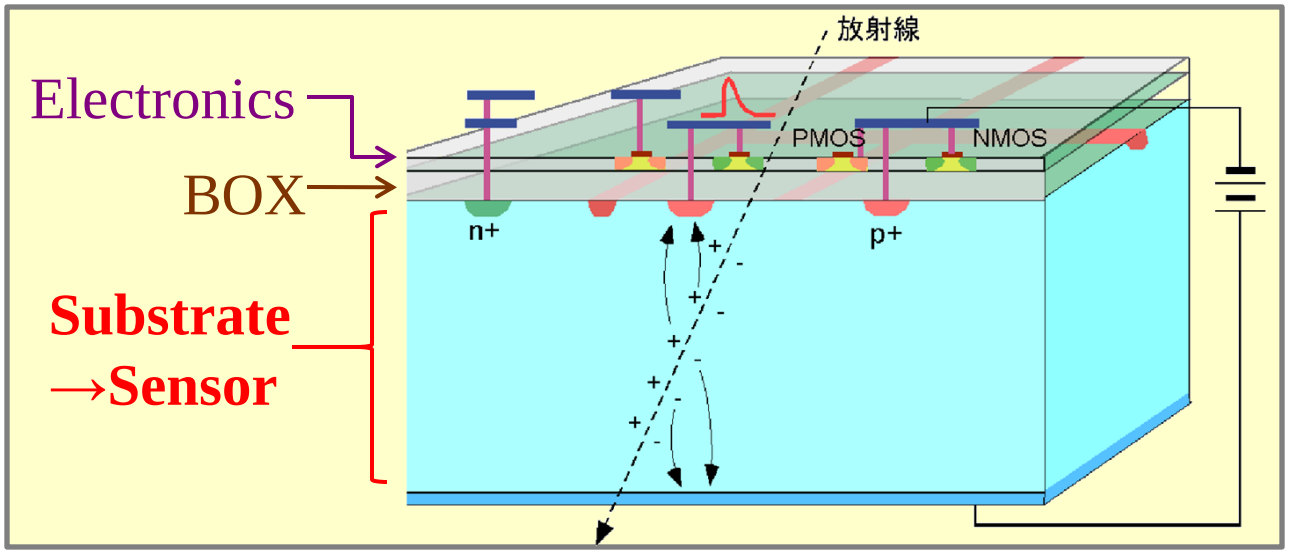


Development of Pair-monitor with SOI technology

The pair-monitor is developed using the SOI technology.

SOI (Silicon On Insulator) pixel detector

- SOI pixel group at KEK is currently developing.
- The sensor and electronics are integrated in the SOI substrate.
  - Monolithic device
  - High speed
  - Low power
  - Thin device
  - Low material



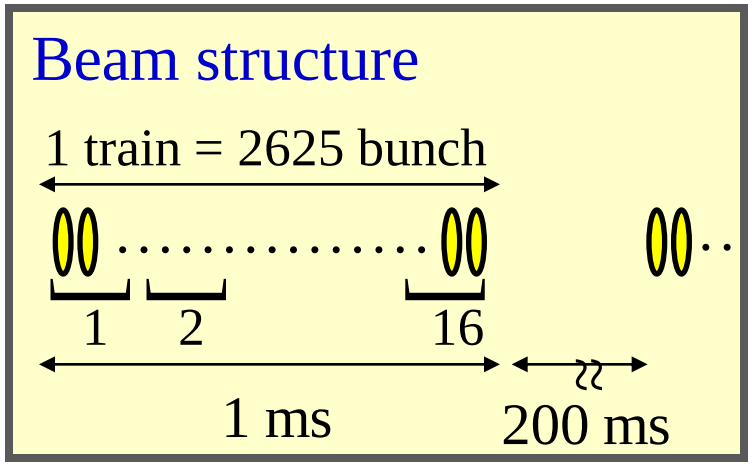
The prototype ASIC for the pair-monitor was fabricated via the MPW Run organized by the SOI pixel group.

- This prototype is not monolithic (Substrate is not a sensor).

Requirement to readout ASIC

Required performance

1. Time resolution : < 260 nsec
   (less than bunch space)
2. Noise level : < 1000 e
   (typical signal level : 15,000 e)
3. Radiation tolerance : > a few Mrad/year
4. Time-dependent measurement
   – Measure the pixel hit count in 16 time slice per train,
   and hit counts are read out during the inter-train gap of 200 ms.

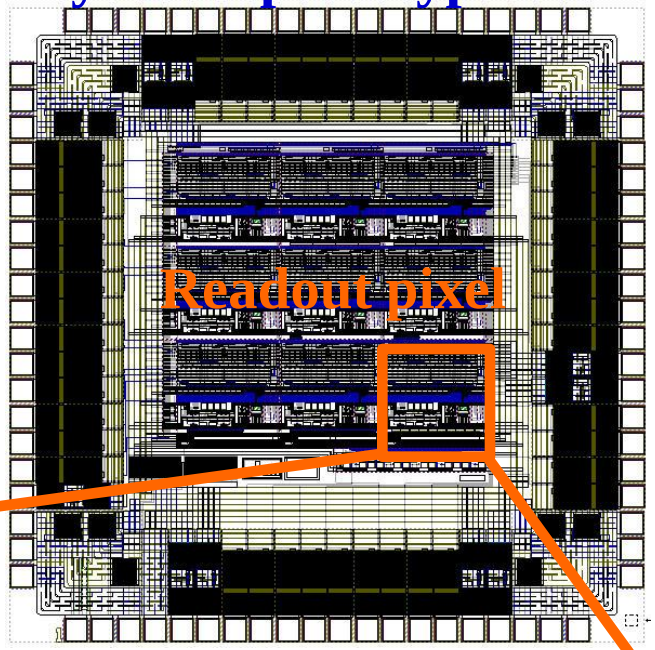


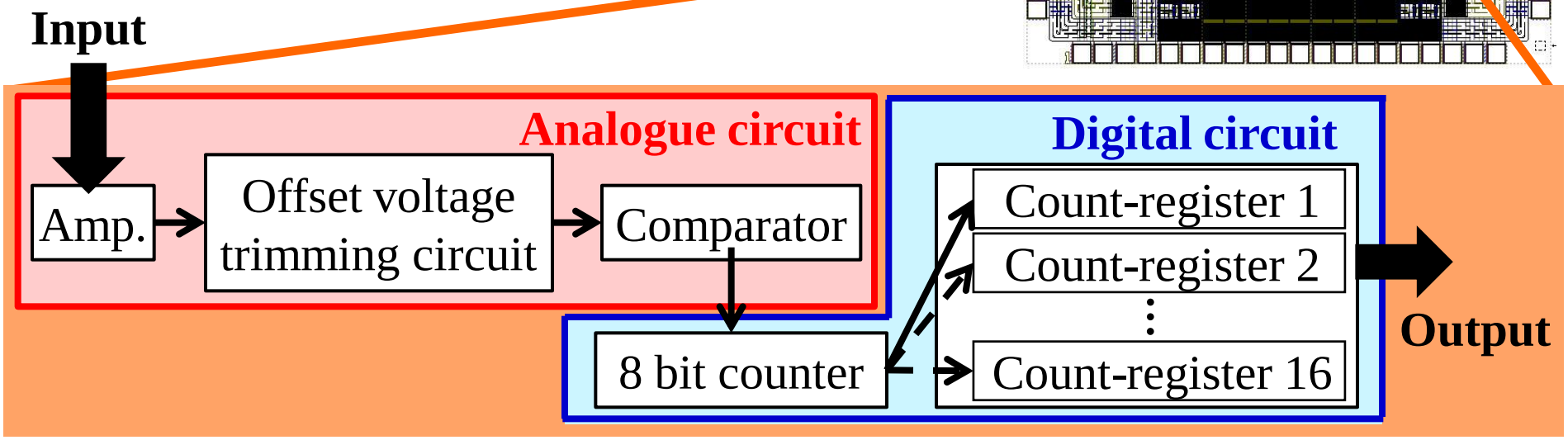
→ The prototype readout ASIC was designed
to satisfy these requirements.

Prototype readout ASIC

- Process : fully depleted-SOI CMOS 0.20 μm
- Chip size : 2.5 x 2.5 mm^2
- # of pixels : 9 (3x3)
- Pixel size : 390 x 350 μm^2
- Each cell has different detector capacitance.

Layout of prototype ASIC





Irradiation test

Irradiation test was performed to test the radiation tolerance and observe the radiation effect.

- X-ray generator : Rigaku FR-D
  - Target : Cu (~ 8 keV)
- Doses : up to 2 Mrad
  - #photons was evaluated by the pin-diode.
  - All the photons are assumed to be absorbed within an attenuation length ($\lambda \sim 66\ \mu m$).
  - Silicon density : d = 2.33 g/cm^3

Radiation effect

There are two types of radiation effect.

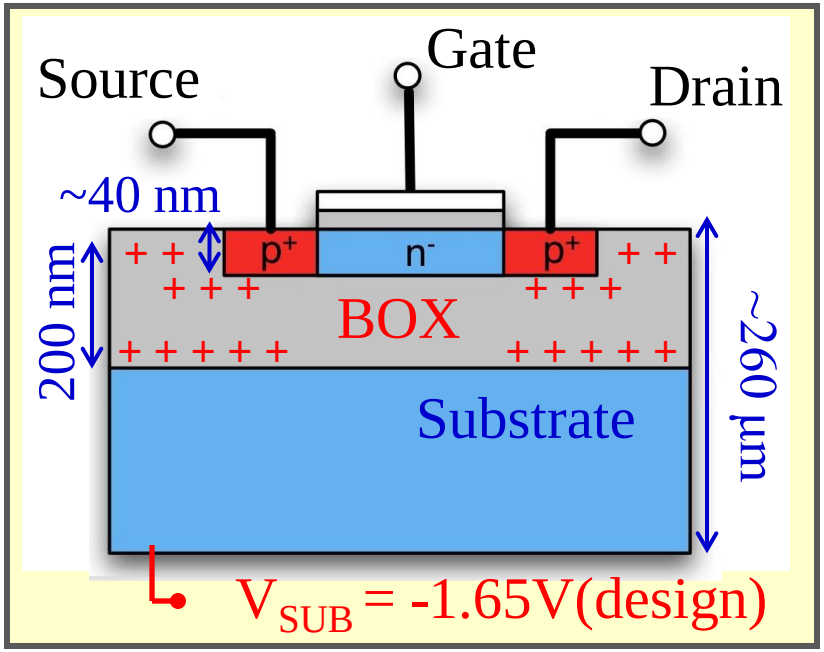
Single event effect (SEE)

- Caused by single energetic particle.

→ SOI device is known as rad-hard for SEE.

Total dose effect (TDE)

- Caused by charge trapped in the oxide layer.



→ Oxide trapped charge could be compensated by the substrate voltage.

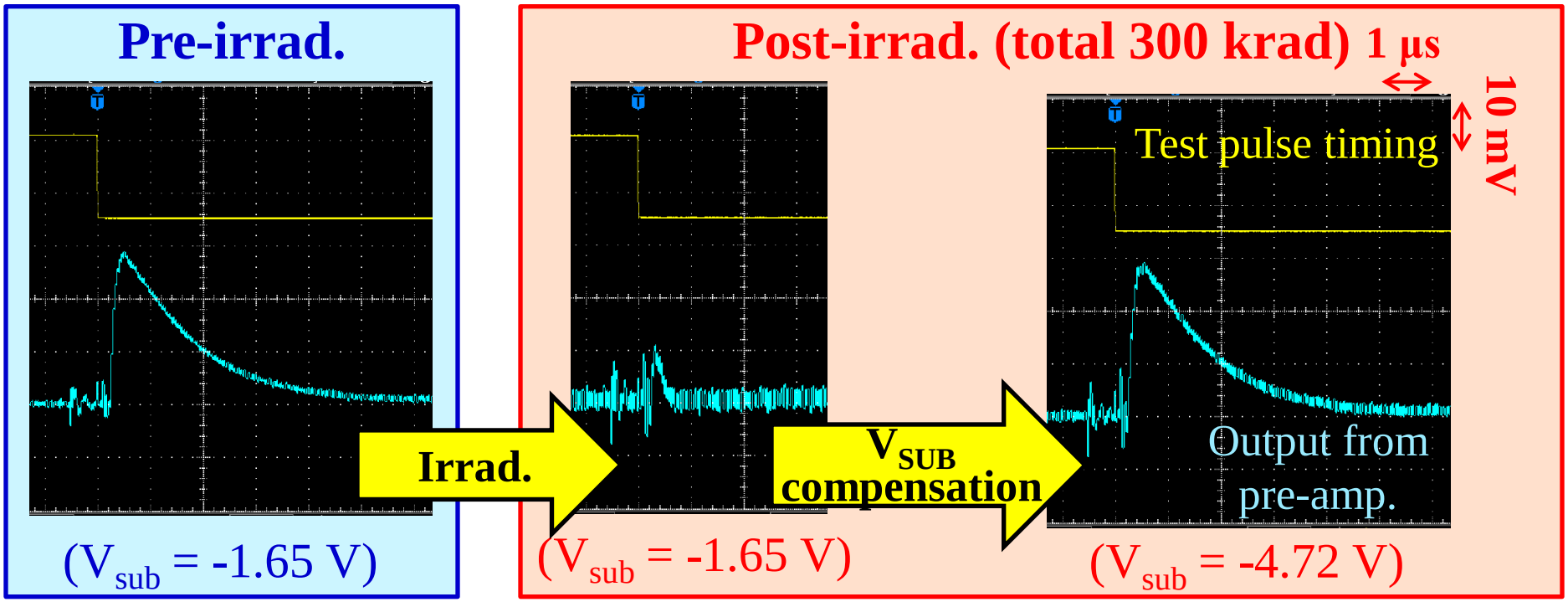
Performed measurements

Signal shape at pre-amp.
Gain
Linearity
Noise level

Signal shape

The signal shape at the pre-amp. was compared.

- By irradiation, the signal shape becomes smaller.



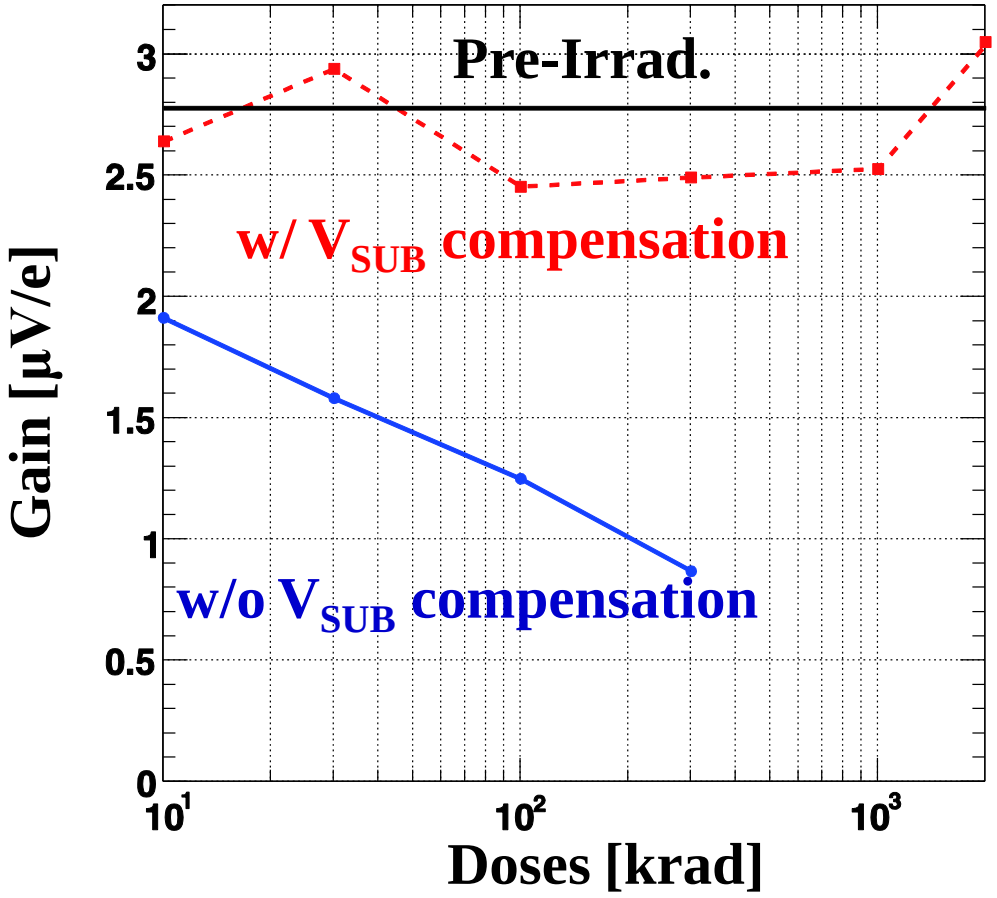
The signal shape of post-irradiation can be returned to that of pre-irradiation by V_{SUB} compensation.

- The transistor was shorted due to large 1 Mrad irradiation, however similarly the signal shape can be returned by V_{SUB}.

Gain

The threshold scan was performed and the gain was compared.

- By the irradiation, the gain becomes smaller.



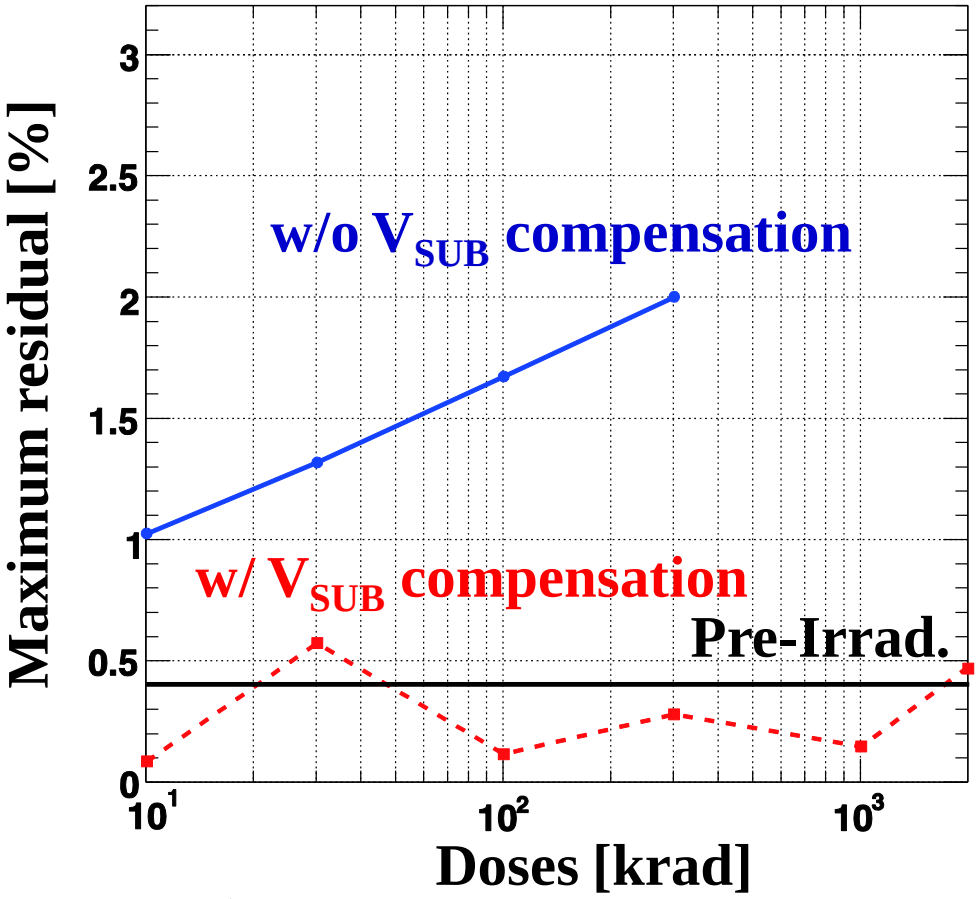
The gain can be restored by V_{SUB} compensation.

Linearity

The threshold scan was performed and the linearity was compared.

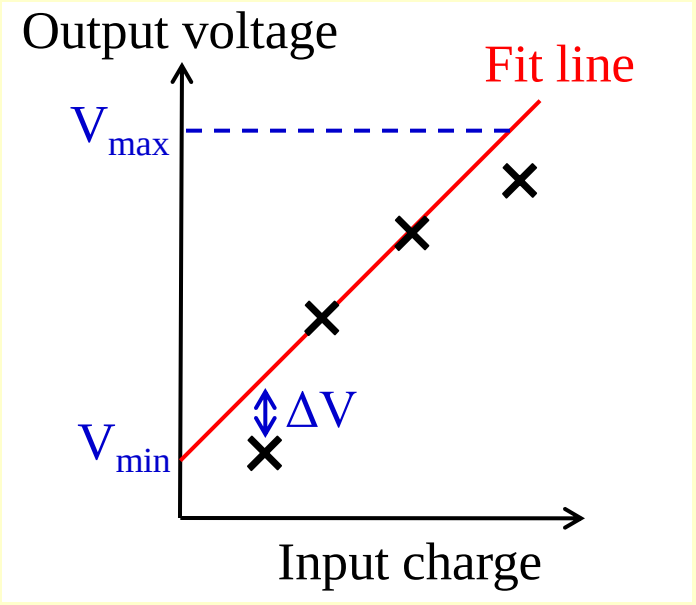
(fitting region : 7,000 ~ 45,000 e)

- By the irradiation, the linearity becomes worse.



Residual

$$\text{Residual}\,[\%] \equiv 100 \times \frac{\Delta V}{V_{max} - V_{min}}$$

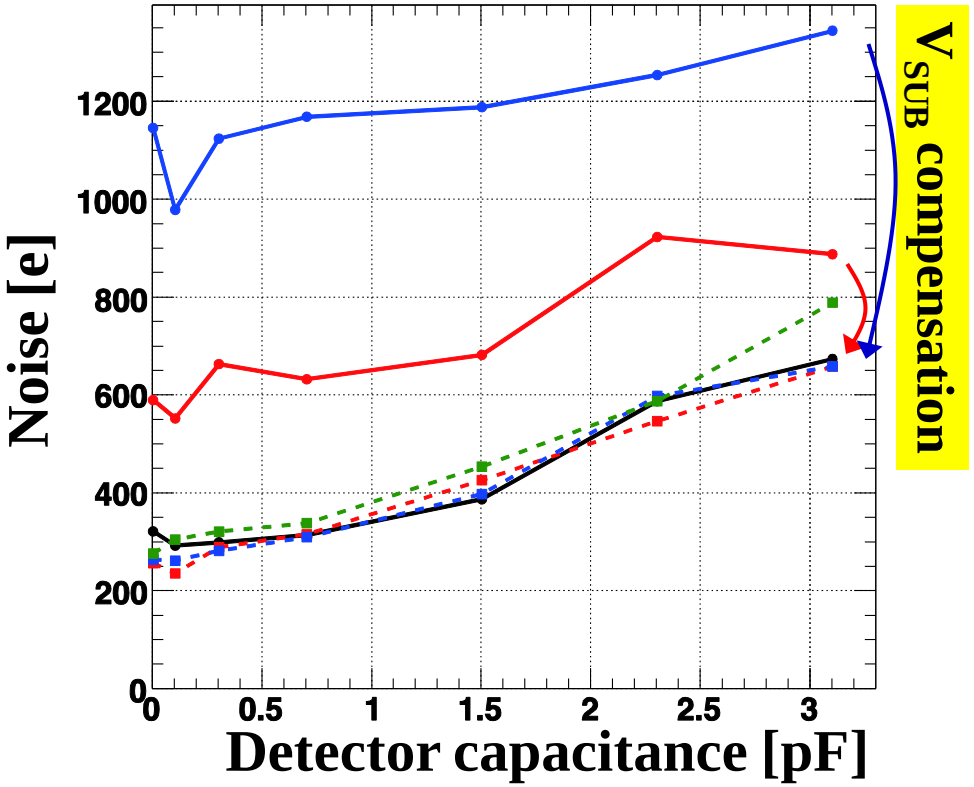


The linearity can be restored by V_{SUB} compensation.

Noise level

The noise level was compared.

- By irradiation, the noise level becomes bigger.



Pre-Irrad.
Post-Irrad. (100krad)
Post-Irrad. (300krad)
Post-Irrad. (2Mrad)

※ Dashed line means w/ V_{SUB} compensation.

The noise level returns to that of pre-irrad. by the V_{SUB} compensation.

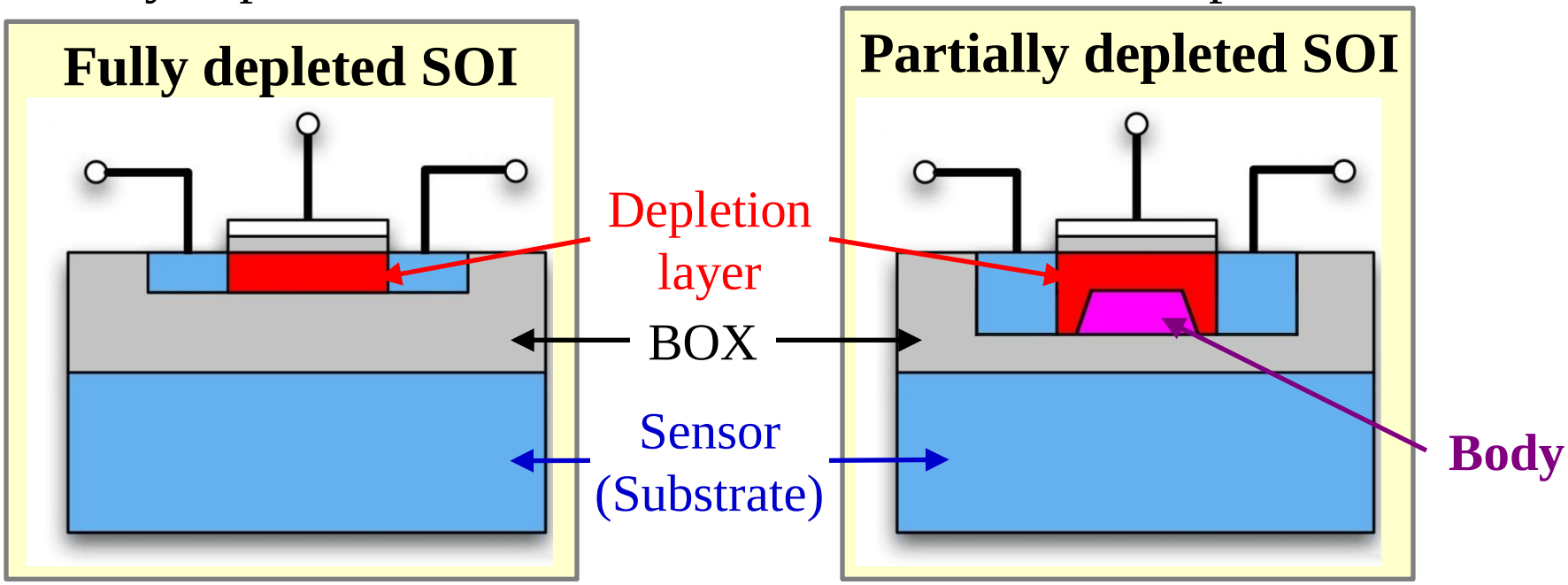
The radiation tolerance up to 2 Mrad was confirmed and oxide trapped charge was compensated by V_{SUB}.

Next prototype

Next prototype is under investigation.

Monolithic

- The V_{sub} compensation can not be used.
- Partially depleted SOI CMOS could be effective to improve rad-hard.



Hybrid

- V_{sub} compensation can be used.

Summary

Pair-monitor is developed with SOI technology.

- The first prototype which is only readout ASIC was produced and the irradiation test were performed successfully.
  - The radiation tolerance up to 2 Mrad was confirmed.
  - The oxide trapped charge was compensated by the substrate voltage.

Plan

- Irradiation test (γ-ray or electron beam)
- Investigation into the next prototype
  - Monolithic or hybrid ?

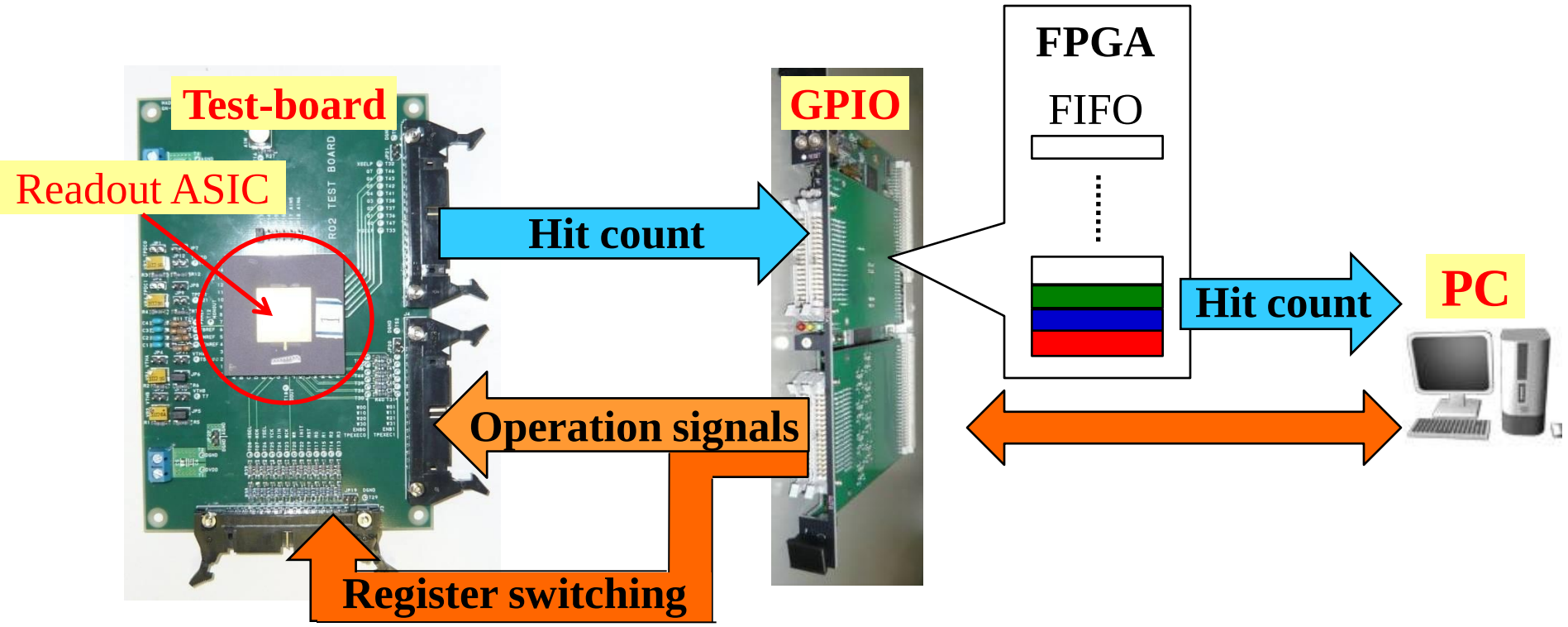
Backup

Test system

The operation test was performed.

Test system

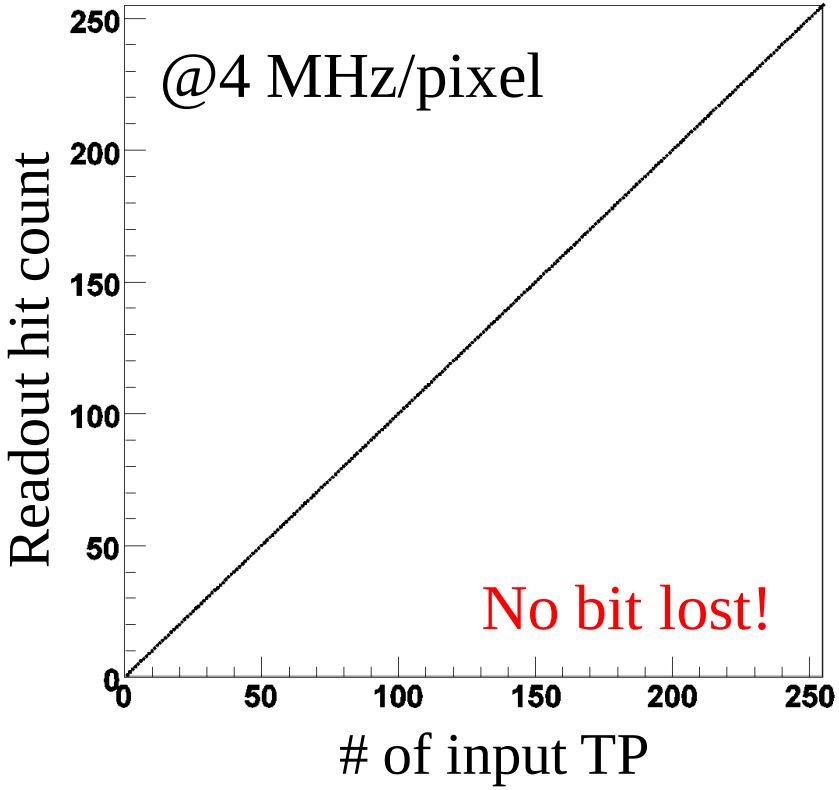
- GNV-250 module was used for the operation and readout .
  - KEK-VME 6U module
- The test-sequence by GPIO is controlled by a PC.



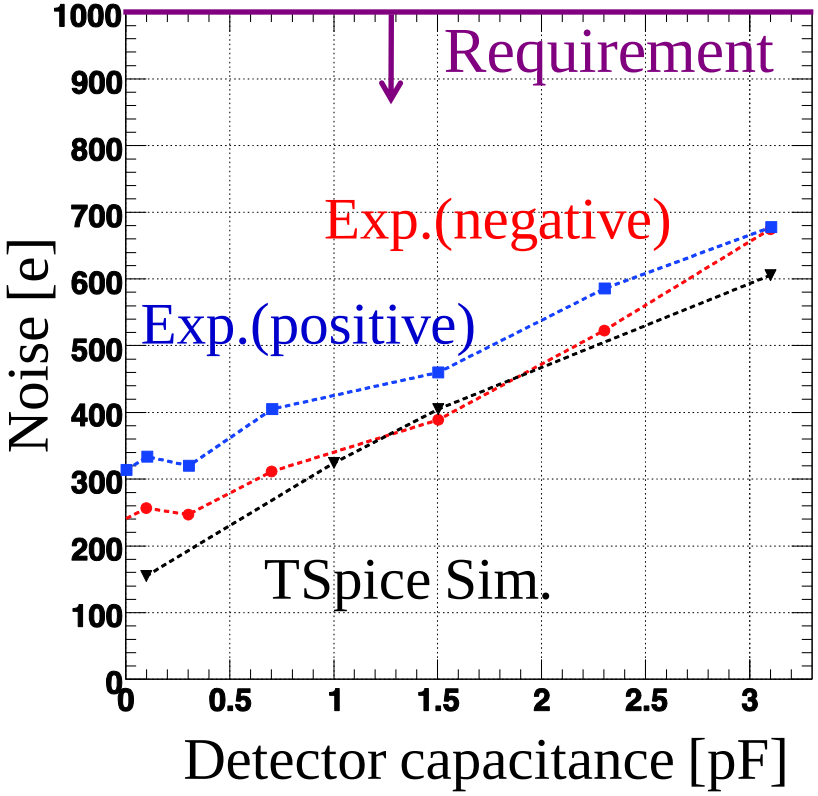
Operation test

Operation test was performed successfully.

Time resolution & Time-dep. measurement



Noise level

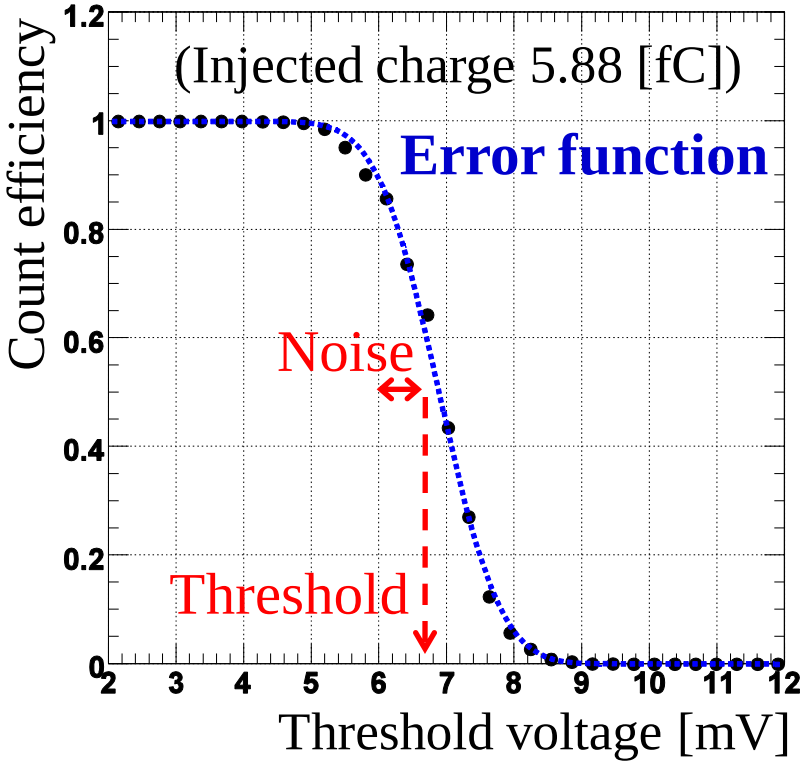


Prototype meets the requirement of time resolution, time-dependent measurement and noise level.

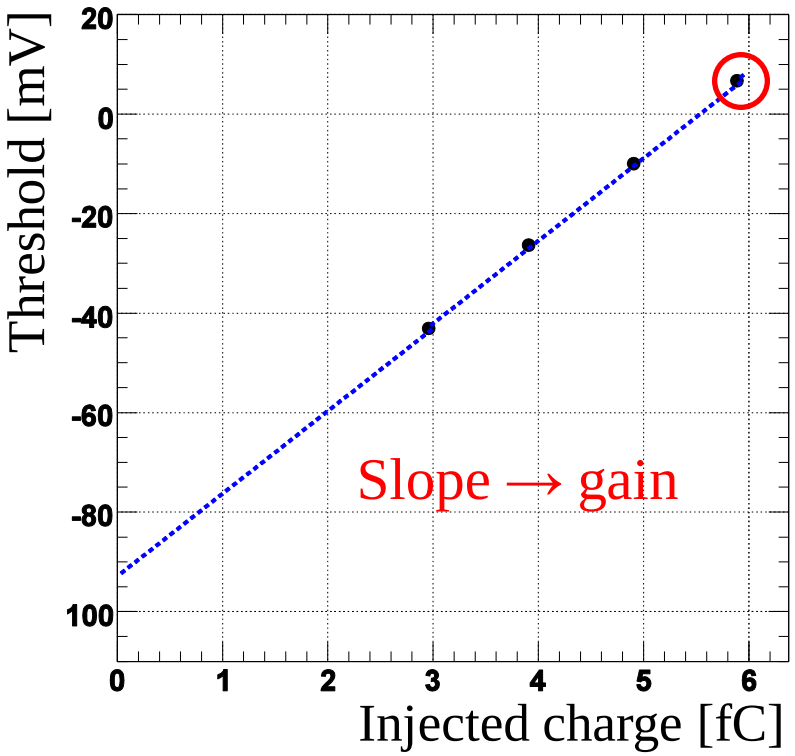
Threshold scan

Threshold scan was performed.

- Fit to error function (S-curve)



The gain was estimated to convert the noise into equivalent noise electrons.



- Threshold : 6.886 ± 0.009 [mV]
- Noise : 0.7152 ± 0.0128 [mV]
- Gain : 16.94 [mV/fC]

Noise : ~260 electrons

Radiation doses

Total Doses = (#photon) × (Doses per a photon)

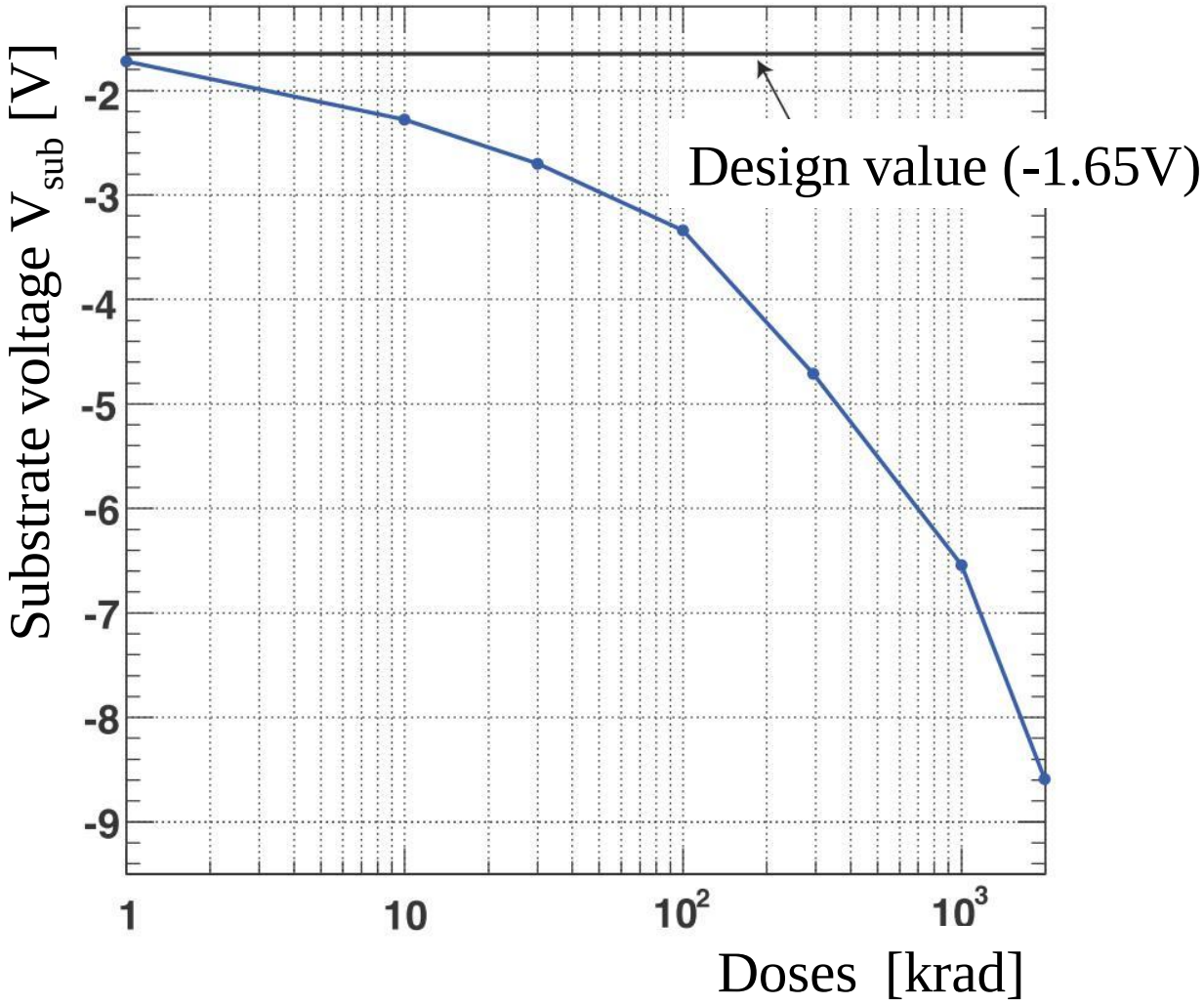
The number of photons

- Evaluated by the photoelectron of diode.
  - $k = 2.5 \times 10^9$ [photon/μA]

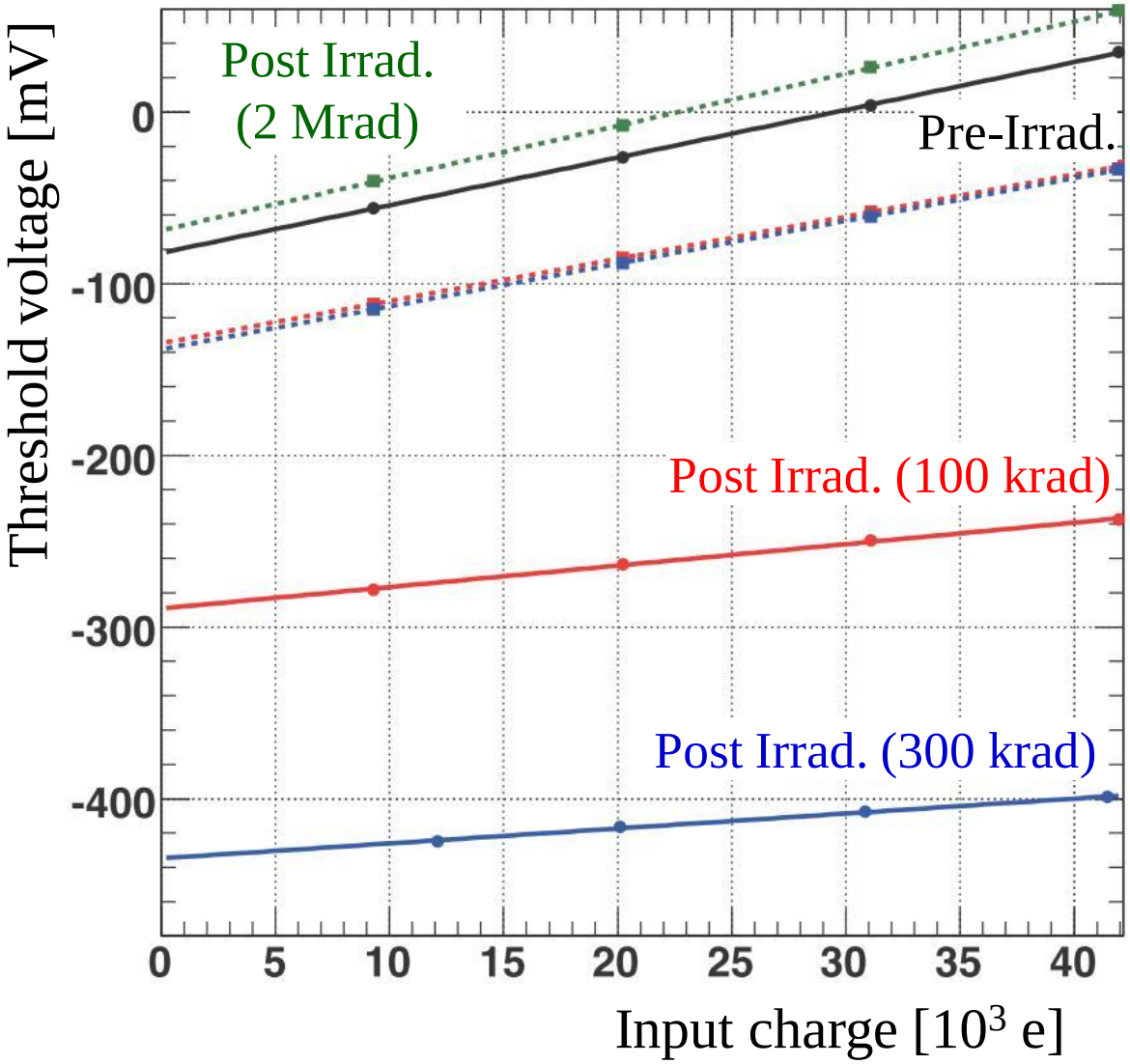
Doses per a photon

- Energy of photon : 8.19 keV
  - Weighted average of Kα (8.04 keV) and Kβ (8.91 keV)
  - All the photons are assumed to be absorbed within an attenuation length ($\lambda \sim 66$ μm)
- Silicon density $d = 2.33$ g/cm^3

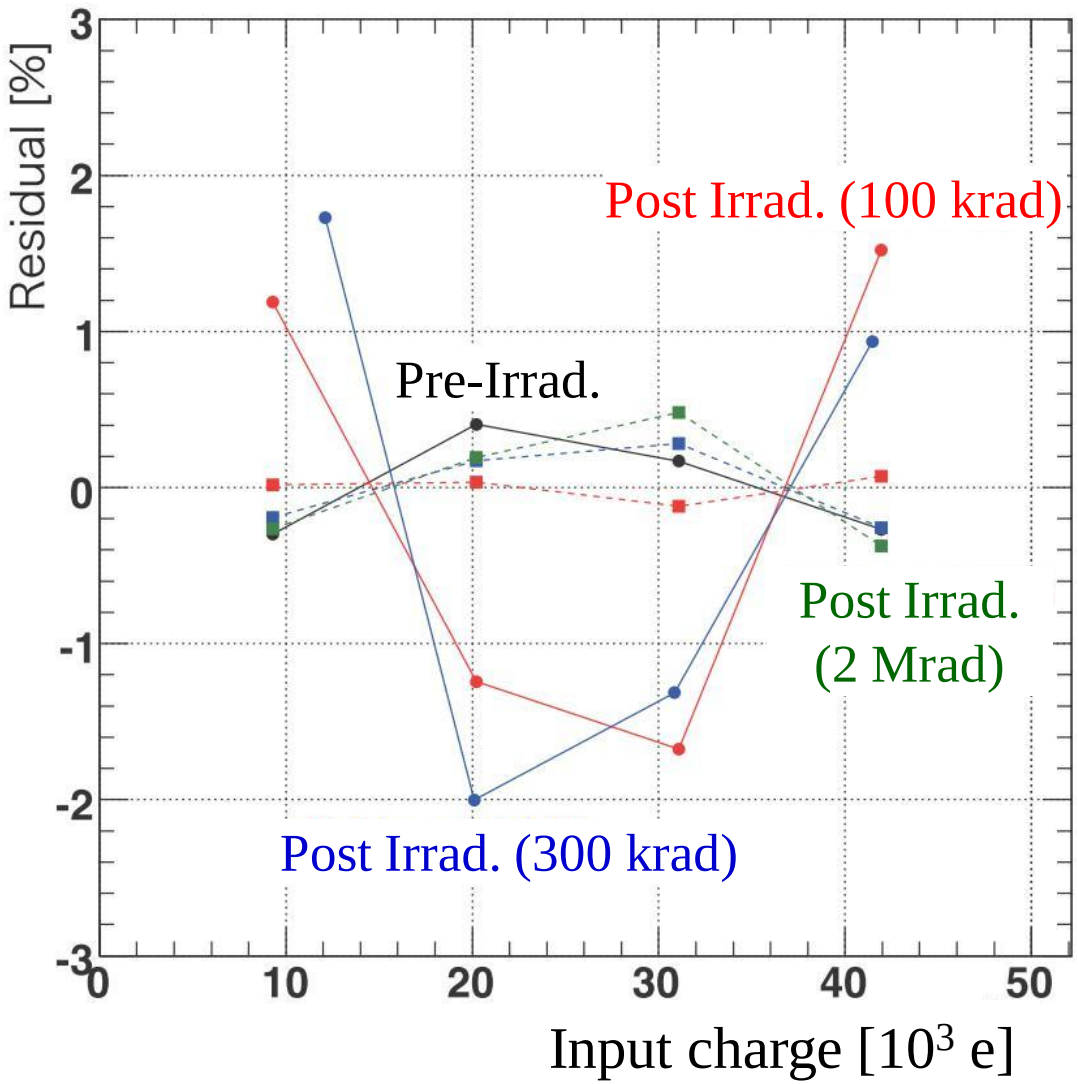
Substrate voltage (V_{sub})



Threshold scan



Residual


Residual [%]
3
2
1
0
-1
-2
-3
0
10
20
30
40
50
Input charge [10^3 e]
Post Irrad. (100 krad)
Pre-Irrad.
Post Irrad.
(2 Mrad)
Post Irrad. (300 krad)