Development of 10 bit pipeline ADC

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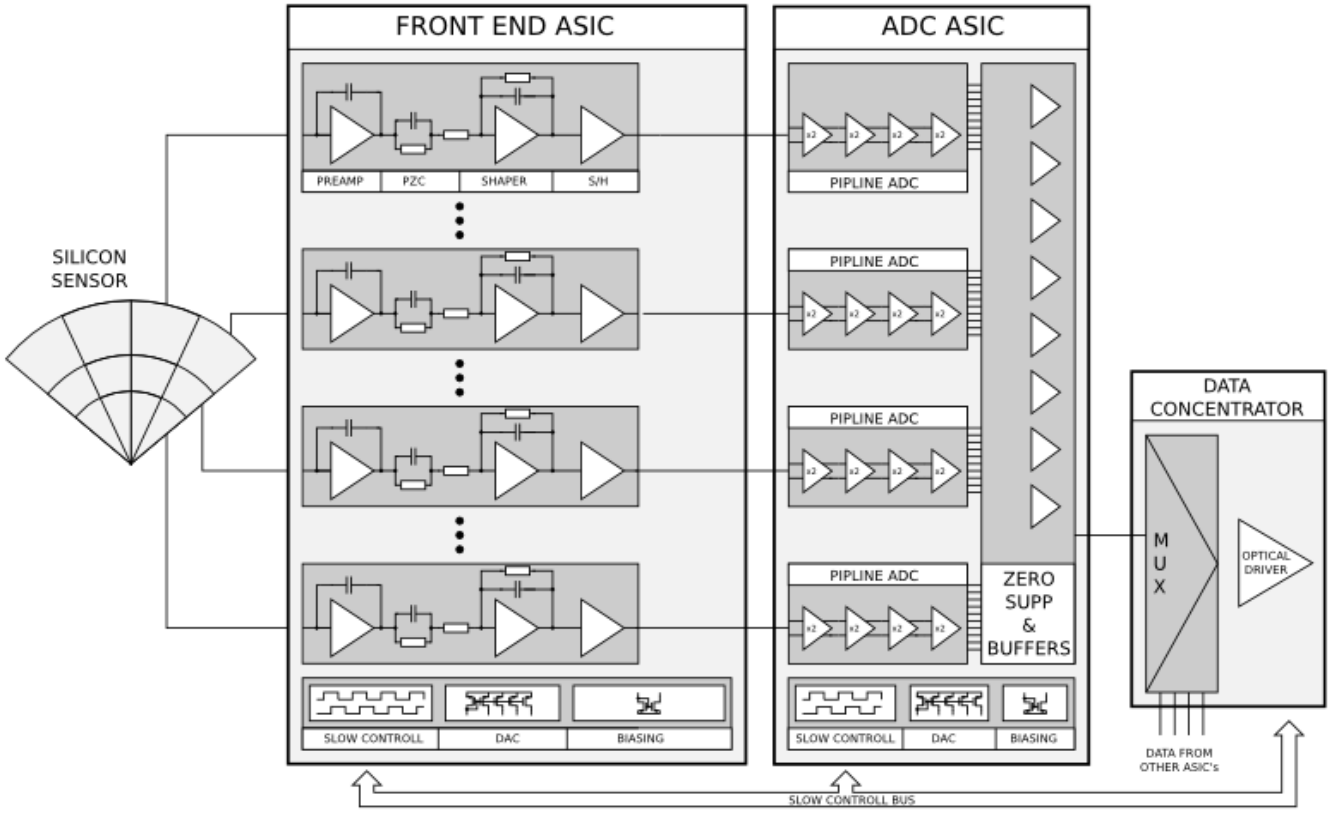
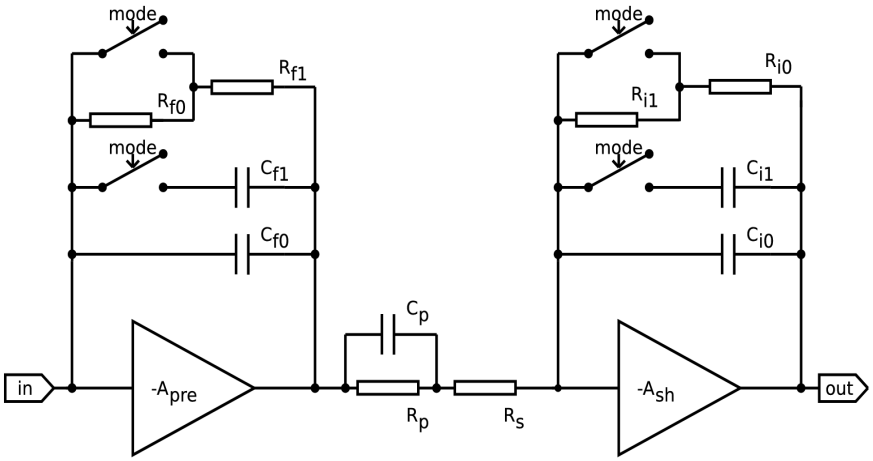
Kraków 12/4/2010

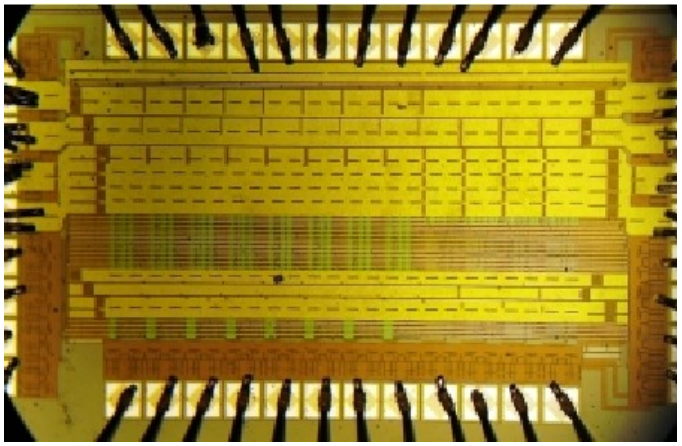
Readout architecture for luminosity detector at ILC

- Prototypes in AMS 0.35 µm
  - 8 channels front-end
  - 1 channel ADC (no zero suppression)

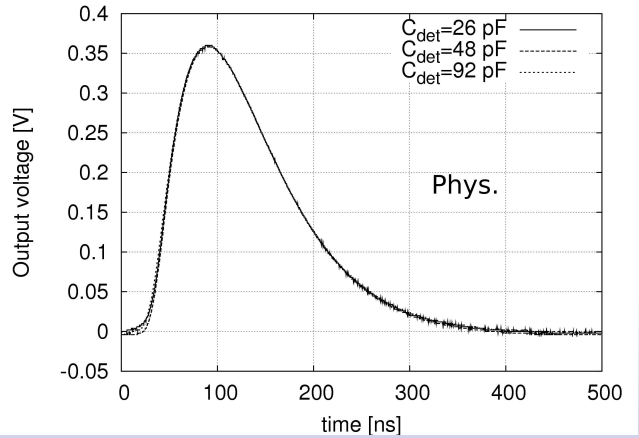


Preamplifier&PZC&Shaper



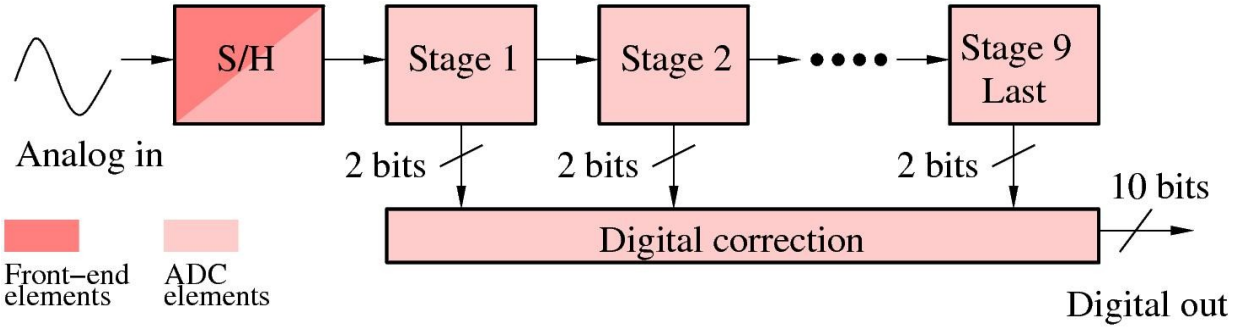


$$\frac{U_{out}(s)}{I_{in}(s)} = \frac{1}{C_f C_i R_s} \cdot \frac{s + 1/C_p R_p}{s + 1/C_f R_f} \cdot \frac{1}{(s + 1/C_i R_i)(s + 1/C_p (R_p \| R_s))}$$

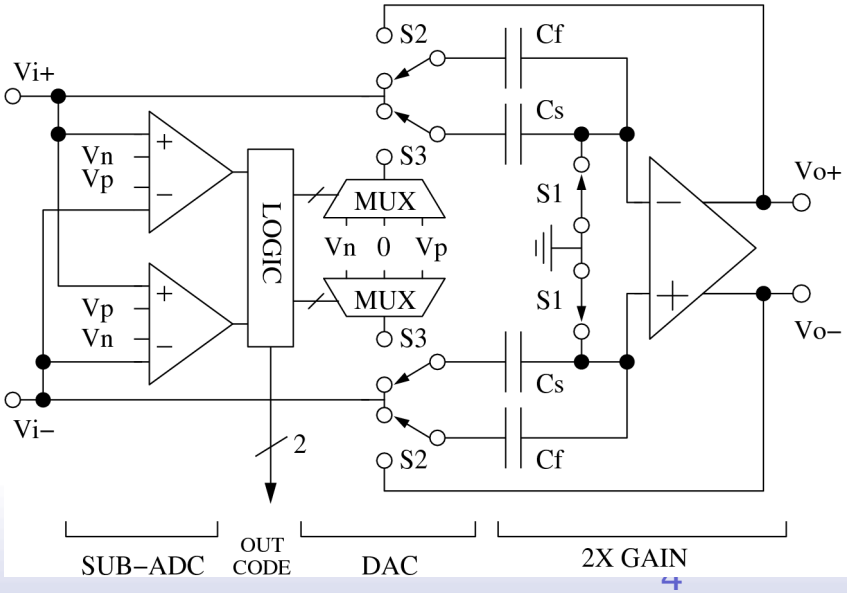


- ASIC with 8 channels
- Variable gain (MIPs and high input charge up to ~ 10pC)
- C_{det} range ~ 0-500 pF
- 1st order shaper T_{peak} ~ 60 ns
- Power consumption < 9 mW/chan

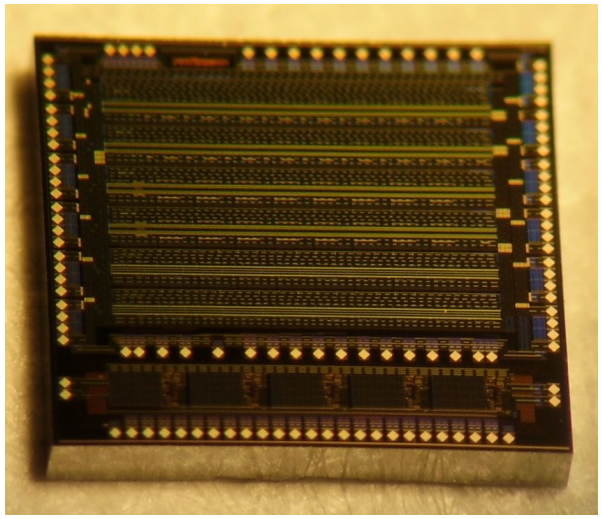
Design of 10 bit pipeline ADC

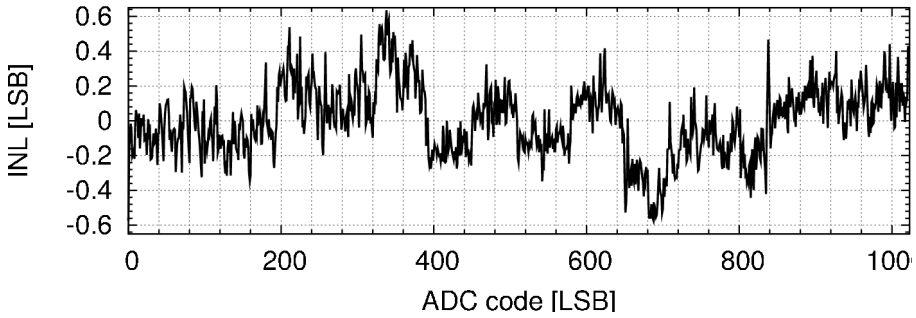


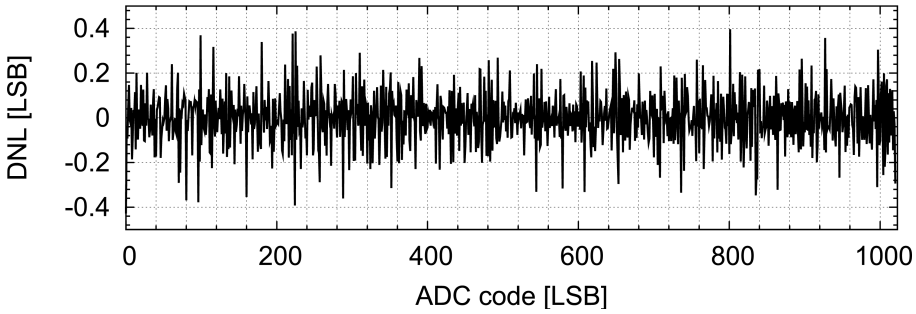
- 10 bit pipeline ADC 1.5 bit/stage
- Variable sampling frequency up to ~25 Ms/s
- Scalable power consumption
- Fully differential
- Power switching OFF/ON (ILC, CLIC beam timing)
- Present version in 0.35 µm AMS, smaller size technology soon...

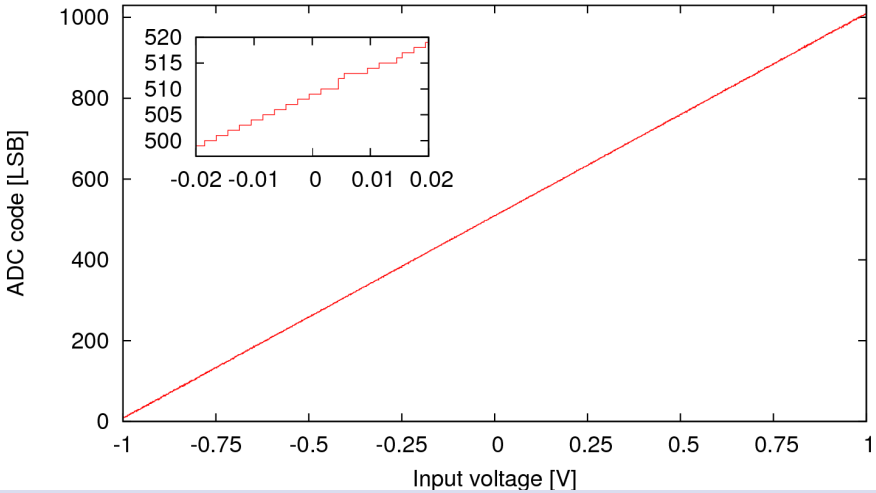


ADC static measurements





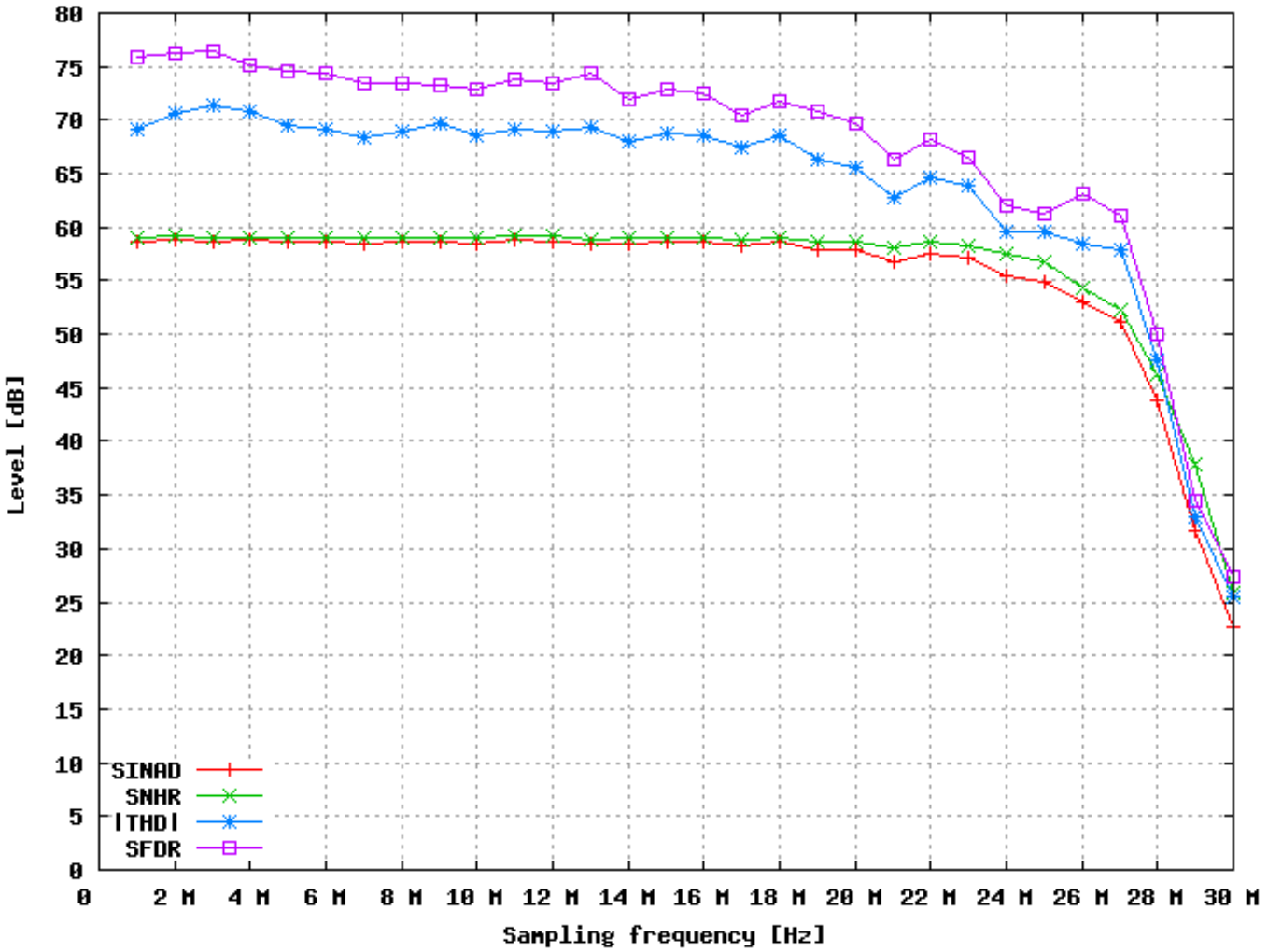




Very good linearity

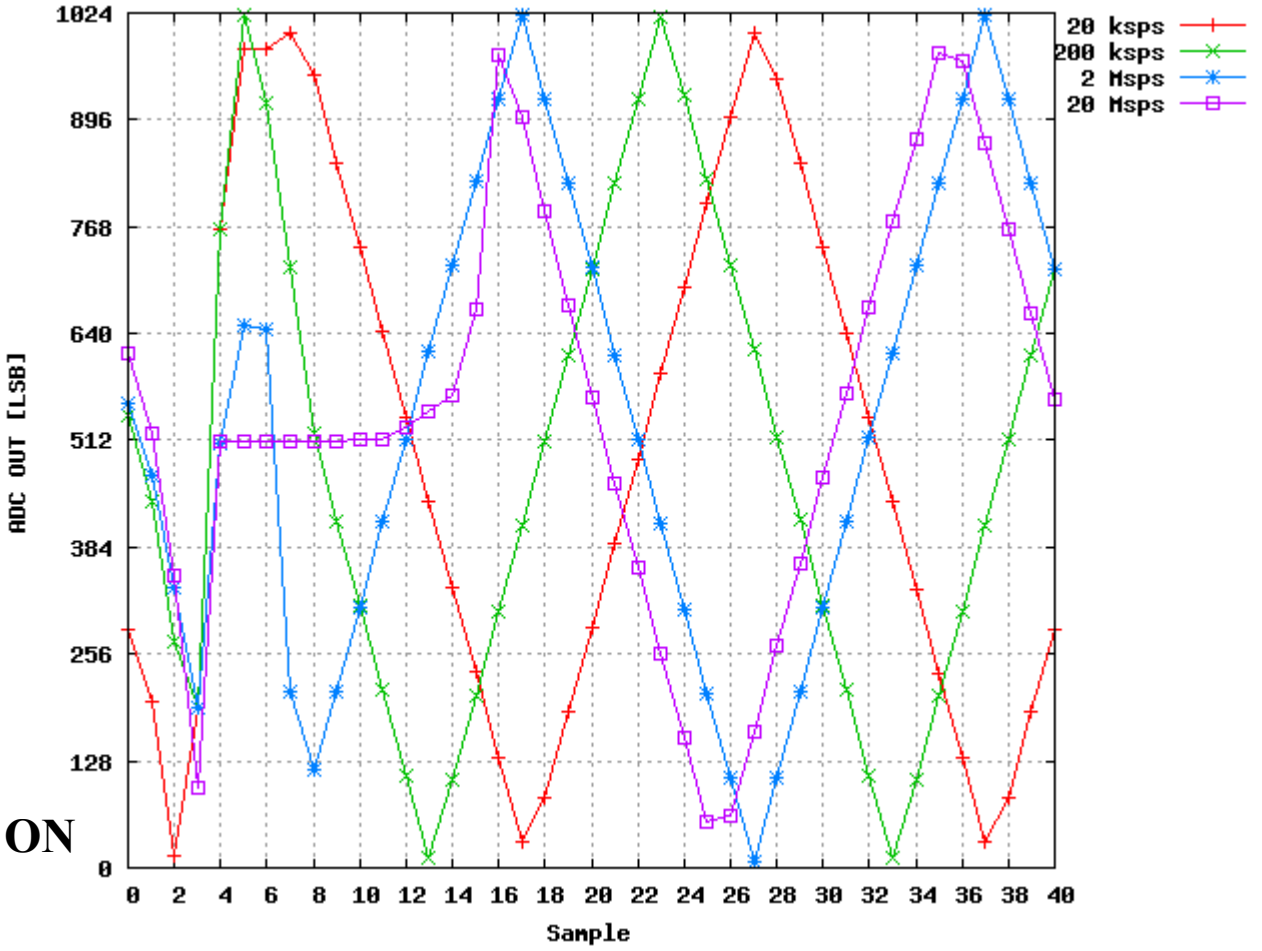
INL < 1LSB, DNL < 0.5 LSB

ADC dynamic measurements



Good dynamic performance ENOB ~ 9.5 bit

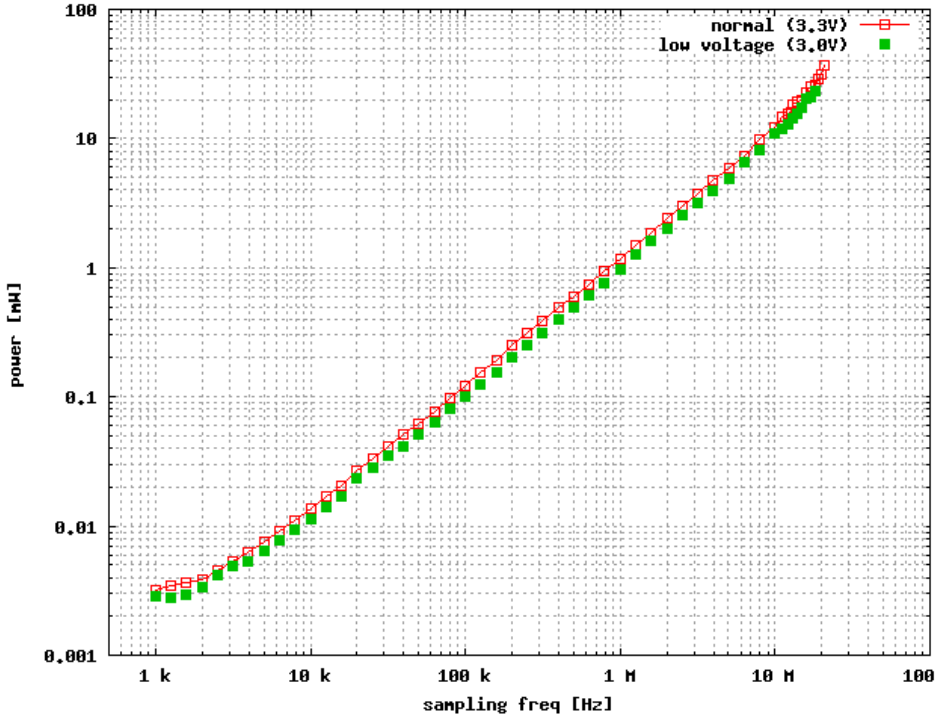
ADC – power OFF/ON

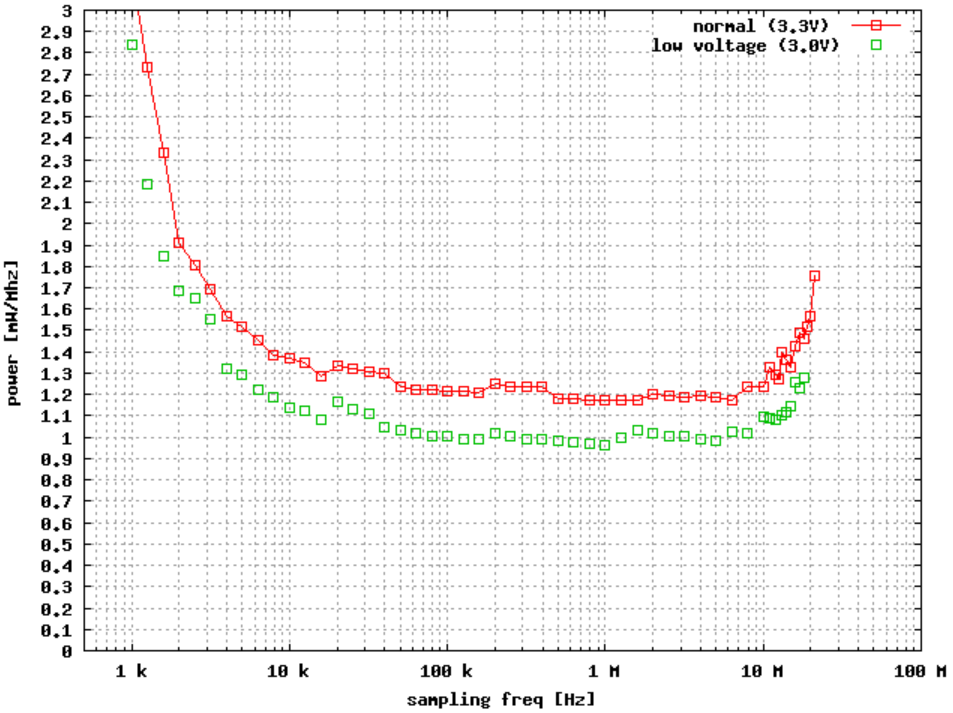


Power ON at t=0

Depending on sampling frequency 8-16 clocks needed for switching ON

ADC power consumption





Presently power consumption about 1-1.5 mW/MHz at worst case (Nyquist input frequency, output buffers)

We have just submitted 8 channels ADC version layout with a pitch 200 µm per channel

Summary

- ADC fully functional and fulfils the requested specifications
- A prototype of the multichannel ADC version should be in cracow in a couple of days...
- Thank you