Contribution ID: **119** Type: **not specified**

Radiation-hard ASICS for sLHC optical data transmission

Saturday 18 July 2009 10:00 (15 minutes)

High-speed data transmission in a high radiation environment poses an immense challenge in the detector design. We investigate the feasibility of using optical links for the silicon trackers of the ATLAS experiment for the planned upgrade of the LHC. The planned upgrade with ten times higher collision rate will produce a similar increase in the radiation. One possibility for the optical transmission is to use VCSEL arrays operating at 850 nm to transmit optical signals while using PIN arrays to convert the optical signals into electrical signals.

We have designed a prototype chip containing building blocks for future SLHC optical links using a 130 nm CMOS 8RF process. The chip contains four main blocks; a VCSEL driver optimized for operation at 640 Mb/s, a VCSEL driver optimized for 3.2 Gb/s, a PIN receiver with a clock/data recovery circuit for operation at 40, 160, and 320 Mb/s, and two clock multipliers designed to operate at 640 Mb/s. The clock multiplier is designed to produce the high speed clock to serialize the data for transmission. All circuitry was designed following test results and guidelines from CERN on radiation tolerant design for the process.

We have irradiated the chips with 24 GeV protons at CERN. For the VDC, the duty cycle of the output signal and the current consumption of the LVDS receiver remained constant during the irradiation. However, we observed significant decreases in the current consumption of the VCSEL driver circuit and the output drive current. This indicated that the think oxide layout used in the VCSEL driver portion of the chip might not be as radiation-hard and the circuit had been redesigned to minimize this sensitivity. For the PIN receiver, we found that the radiation produced no significant degradation, including the single event upset rate. The upset rate decreased with larger PIN current and was higher for a chip coupled to a PIN diode as expected. For the clock multipliers, we observed that the clocks of some chips lost lock during the irradiation and power cycling was needed to resume operation at 640 MHz. We will present the results from the detailed characterization of the irradiated chips.

Author: Prof. GAN, K.K. (The Ohio State University)

Presenter: Prof. GAN, K.K. (The Ohio State University)

Session Classification: IV. Detectors (LHC and R&D) and Accelerators

Track Classification: Detectors (LHC and R&D) and Accelerators