Performance of the ALIBAVA system with irradiated and non-irradiated microstrip silicon sensors

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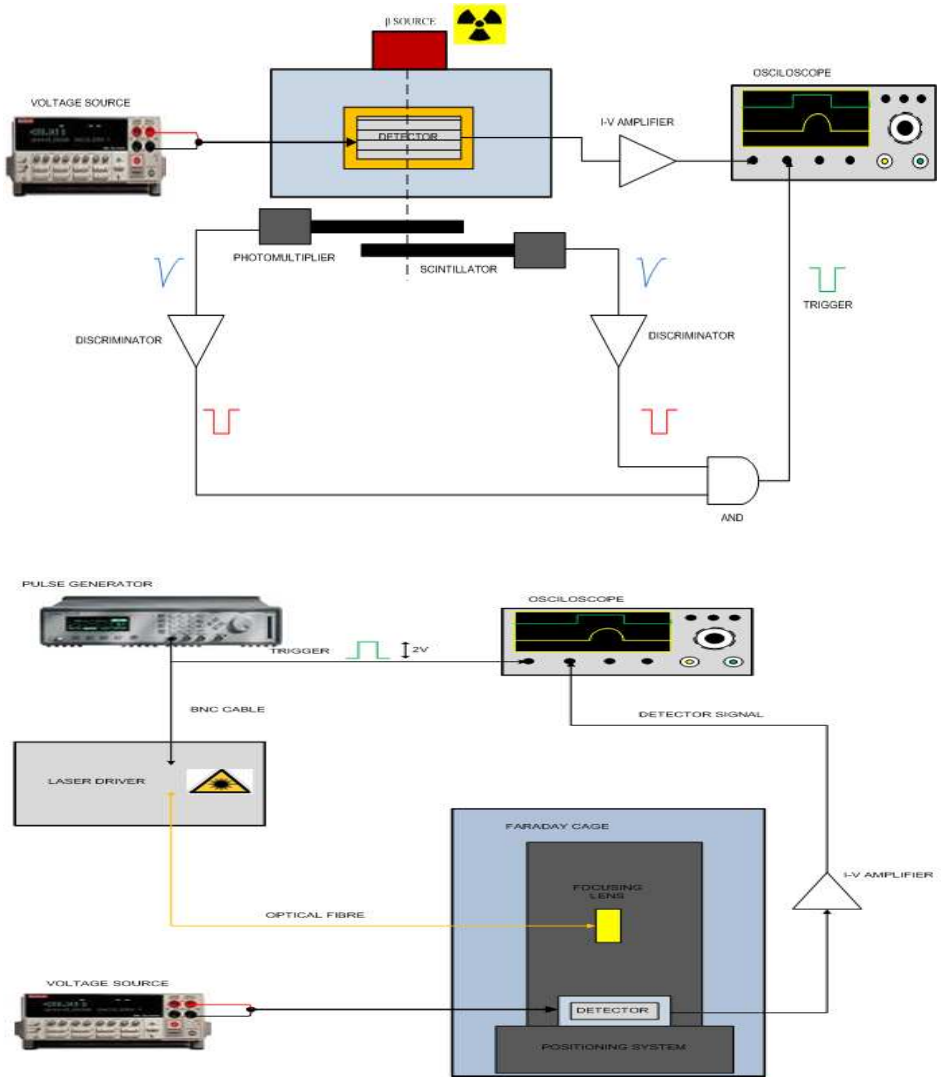
Outline

- Motivations.
- Main system characteristics.
- System architecture.
  - Daughter board.
  - Mother board.
  - PC software.
- Processing of acquired data.
- Measurements with non-irradiated detectors.
- Measurements with irradiated detectors.
- Charge collection measurements.
- Summary.

Motivations

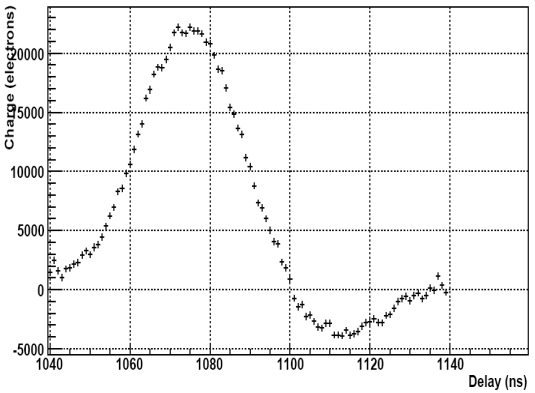
- Study the main properties of highly irradiated microstrip silicon sensors: SLHC.
- Particularly the collected charge: detector performance.
- Difficulty for obtaining this type of measurements:
  - Required equipment is expensive.
  - A large number of channels has to be measured.
  - There is minimum standardization.
- Testing with an electronic system as similar as possible to those used at LHC experiments: a LHC front end readout chip should be used.
- Analogue readout is preferred for accurate pulse shape reconstruction.



Main system characteristics

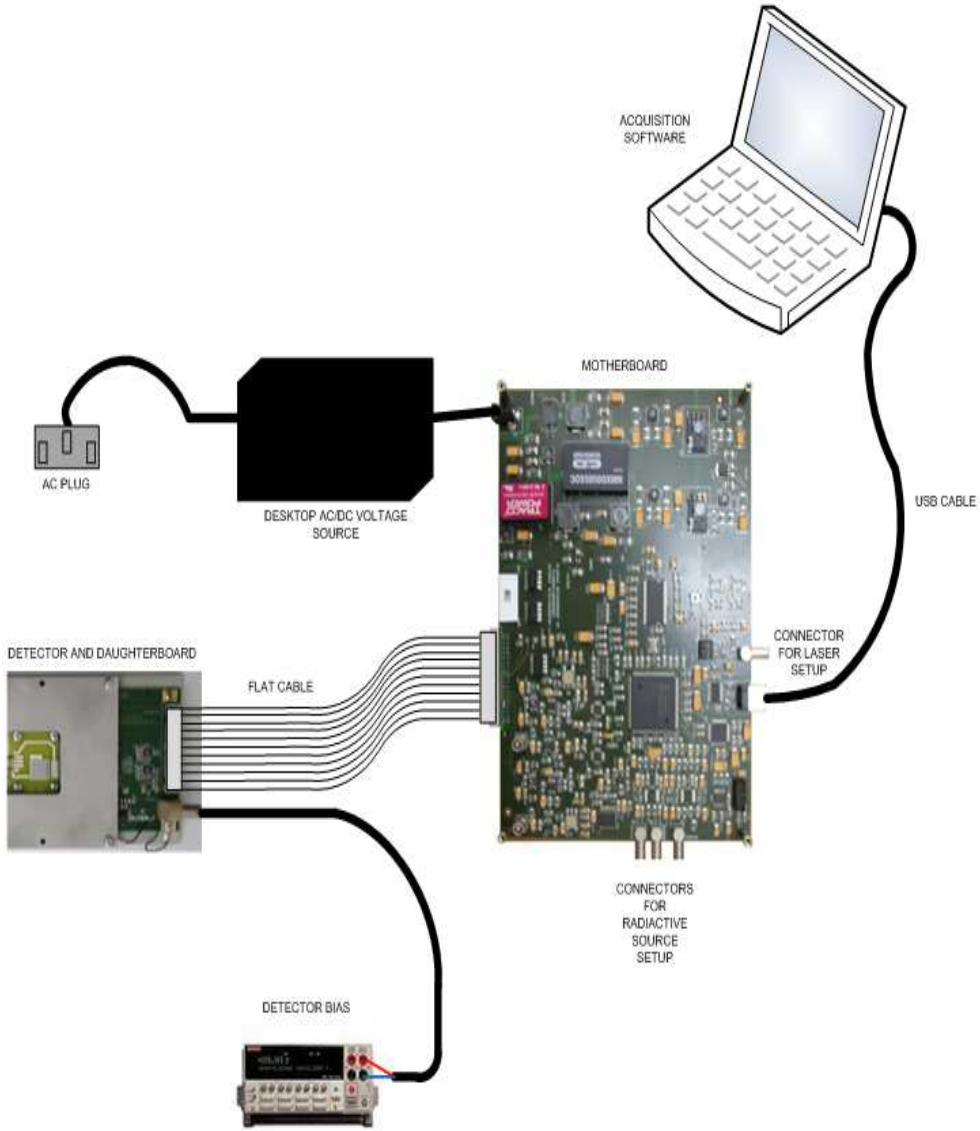
- A compact and portable system.
- The system can be used with two different laboratory setups:
  - Radioactive source: external trigger input from one or two photomultipliers.
  - Laser system: synchronized trigger output generated internally for pulsing an external excitation source.
- The system contains two front-end readout chips (Beetle chip used in LHCb) to acquire the detector signals.
- USB communication with a PC which will store and will process the data acquired.
- System control from a PC software application in communication with a FPGA which will interpret and will execute the orders.
- Own supply system from AC mains.

The main goal is reconstructing the analogue pulse shape from the readout chip front-end with the highest fidelity from the acquired data.



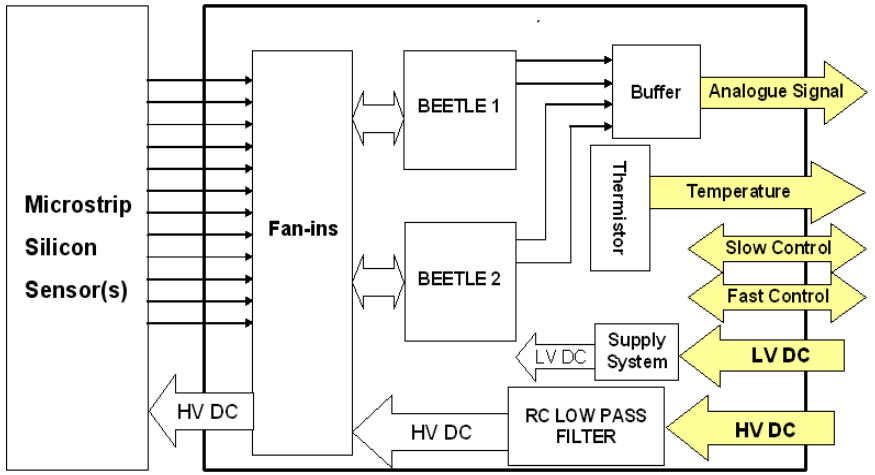
System architecture

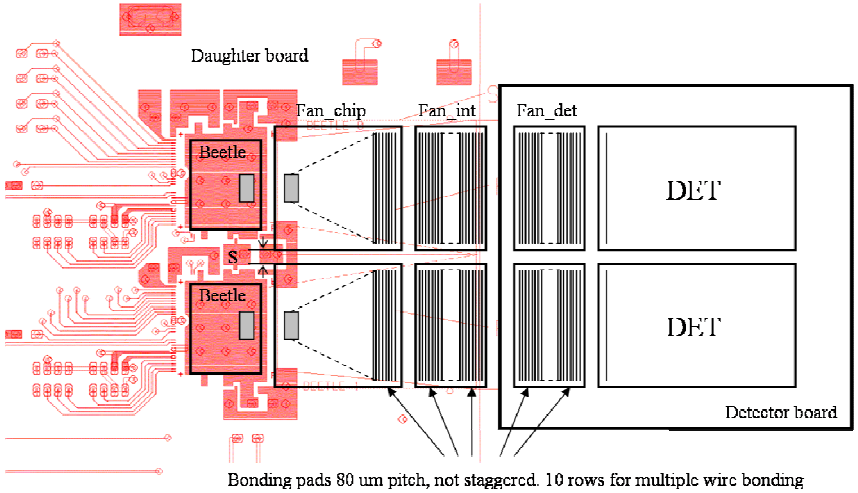
- Software part (PC) and hardware part connected by USB.
- **Hardware part**: a dual board based system connected by flat cable.
  - **Mother board** intended:
    - To process the analogue data that comes from the readout chips.
    - To process the trigger input signal in case of radioactive source setup or to generate a trigger signal if a laser setup is used.
    - To control the hardware part.
    - To communicate with a PC via USB.
  - **Daughter board** :
    - It is a small board.
    - It contains two Beetle readout chips
    - It has fan-ins and detector support to interface the sensors.
- **Software part**:
  - It controls the whole system (configuration, calibration and acquisition).
  - It generates an output file for further data processing.

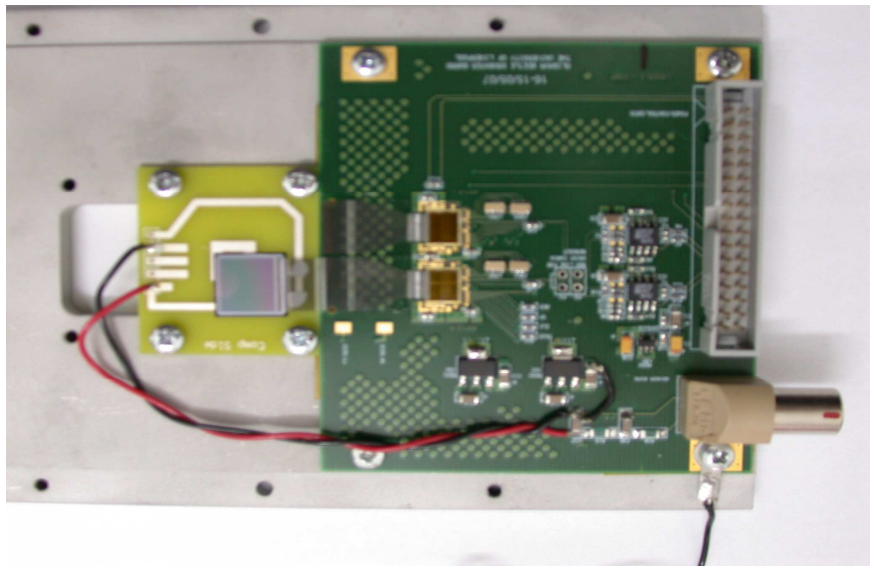


Daughter board

- Two Beetle readout chips in parallel mode.
  - 256 input channels.
  - Analogue front-end with 25 ns of peaking time.
  - Analogue multiplexed readout of each chip.
  - Output dynamic range ~ ±110000 electrons.
- Buffer stage for sending the analogue output signals to the mother board.
- Control signals provided by the mother board and shared by both Beetle chips.
- A thermistor (NTC) for sensing the temperature close the Beetle chips.
- Low voltage DC level (5 V) for Beetle chips (2.5 V) and buffer stage power supply (3 V): provided by the motherboard.
- High voltage DC level for silicon detector(s) bias: external power supply.
- Fan-ins and detector board: multiple wire bonding and two different sensor sizes.

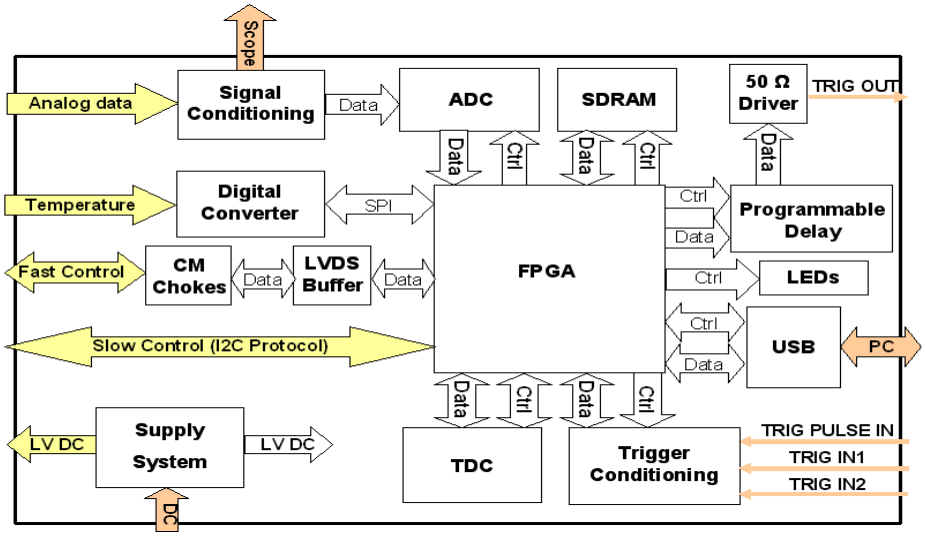


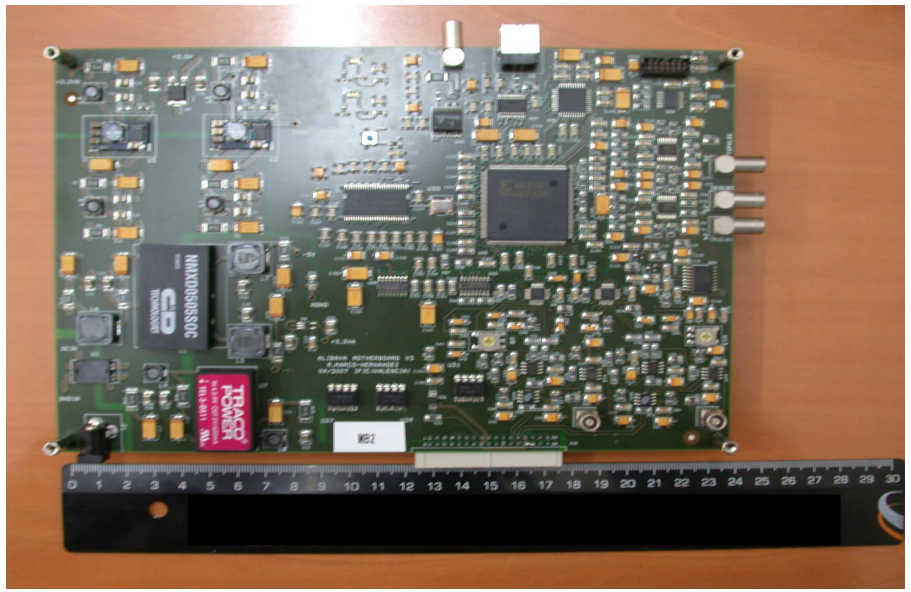




Mother board

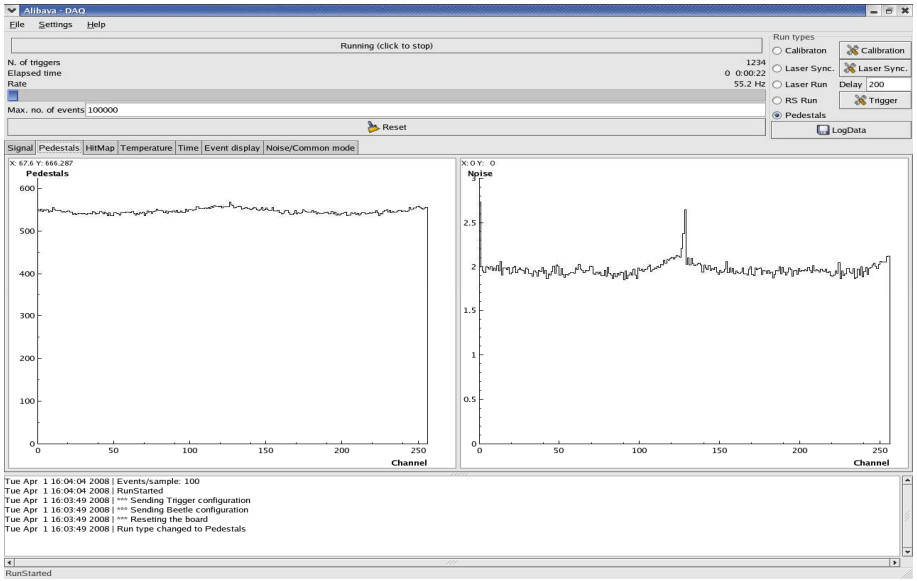
- Analogue signal conditioning:
  - Amplification and filtering: minimization of noise.
  - Buffering: two copies of the Beetle multiplexed analogue outputs for spying with a scope
- ADC: digitalization at 40 MSps of the Beelte analogue multiplexed signals.
- Digital converter: temperature analogue signal digitalization.
- Generation of control signals for Beetle chips by FPGA: DAQ sequences and configuration.
- Trigger conditioning and TDC for obtaining a time stamp of each trigger with radioactive source setup.
- Generation of a trigger output with programmable delay for the laser source.
- USB controller.
- SDRAM (512 Mb) for temporal storage of acquired data.
- FPGA (40 MHz): custom logic and embedded µP.
  - Control of the hardware.
  - Synchronization of DAQ sequences.
  - Generation of Beetle control signals.
  - Communication with the software.
- Supply system: from AC/DC desktop power supply (5V).
  - Generation of MB and DB supply levels.

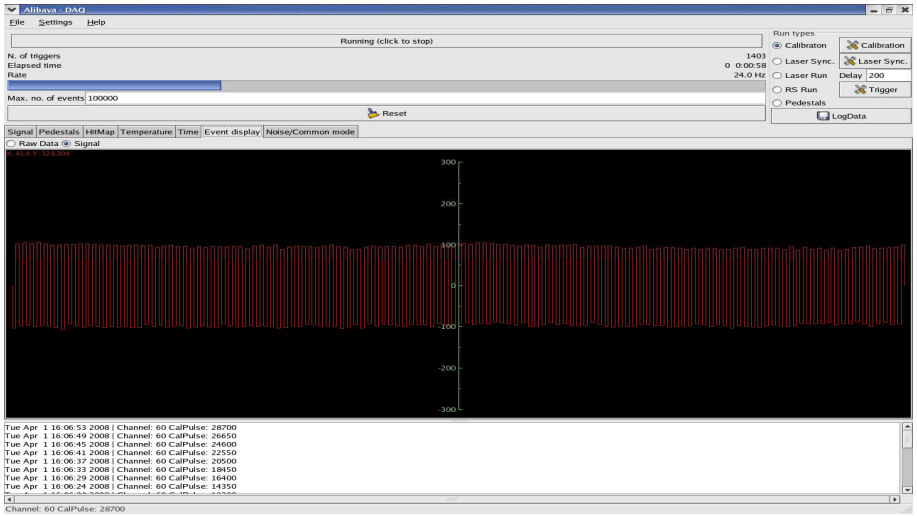




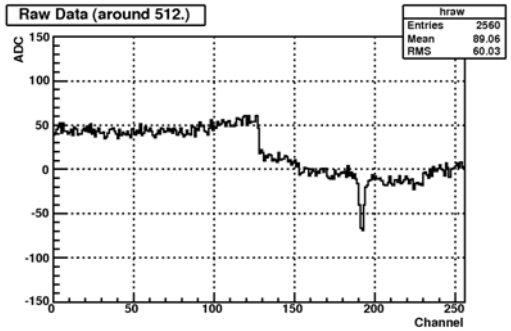
PC software

- Functions:
  - Control the whole system (configuration, calibration and acquisition).
  - Processing and monitoring of acquired data.
  - User interface with the system (GUI).
  - Generation of information (output files).
- Two software levels:
  - Low level:
    - Software/mother board communication by USB: VCP (virtual com port) driver (2.4 Mb/s) used.
    - Processing of acquired data.
  - High level:
    - GUI: control of the system and data monitoring.
    - Output file generation for further processing and analysis.
- Programmed in C++.
- Operating system compatibility:
  - Linux version fully operational.
  - Maybe Windows in the future.
- There are also macros for ROOT in order to process the data acquired with the software.



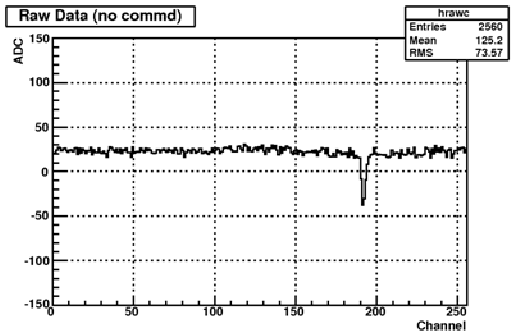


Processing of the acquired data



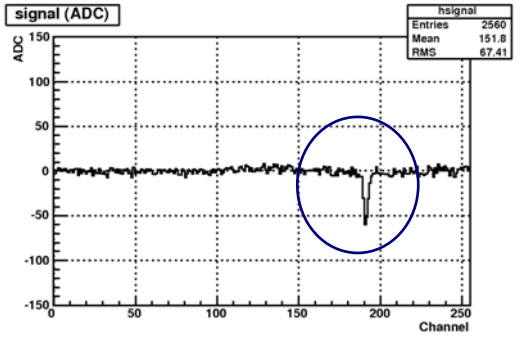
Raw data (ADC counts vs channel number): digitalization of the Beetle analogue multiplexed output signal

Pedestals correction



Raw data with pedestal value for each channel corrected (ADC counts vs channel number)

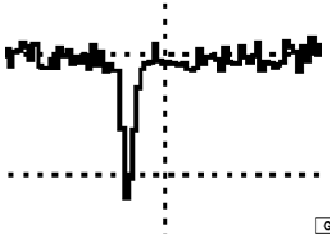
Common mode correction



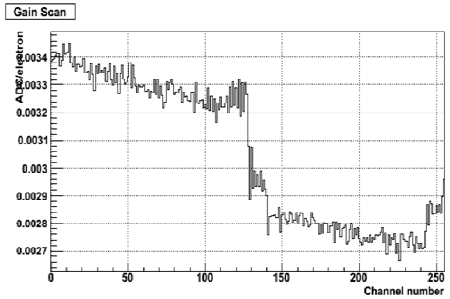
Signal corresponding to an event (trigger): ADC counts vs channel number

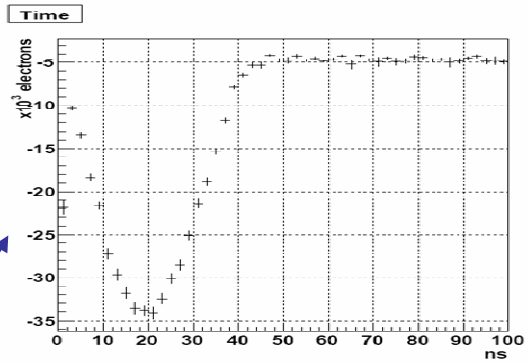
Signal computation of acquired data from each trigger

Signal is computed as the sum of strips in a cluster.
➔Feed S/N > 6.
➔Neighbours S/N > 2.5.

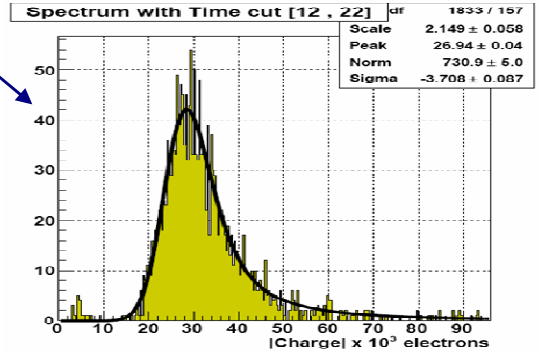


We can obtain different representations of acquired data from a given number of triggers. We use the calibration data for ADC counts to electrons conversion





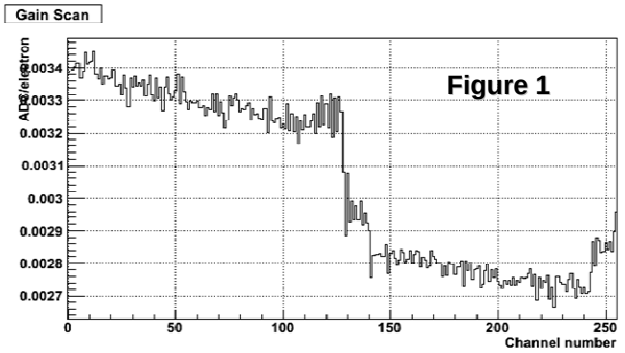
Pulse shape reconstruction: collected charge (electrons) vs. delay (ns)

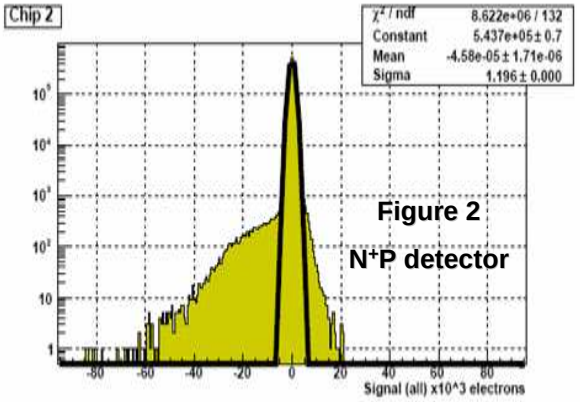


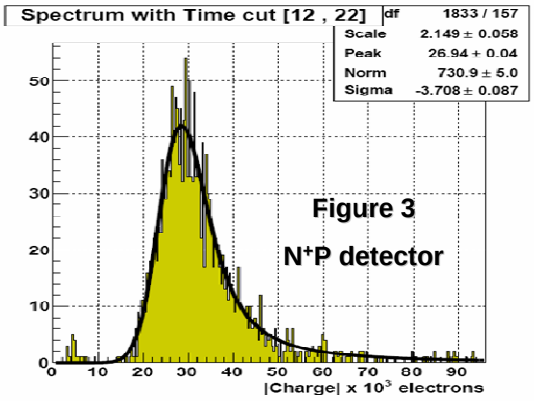
Signal spectrum with a time cut: number of events vs. collected charge (electrons)

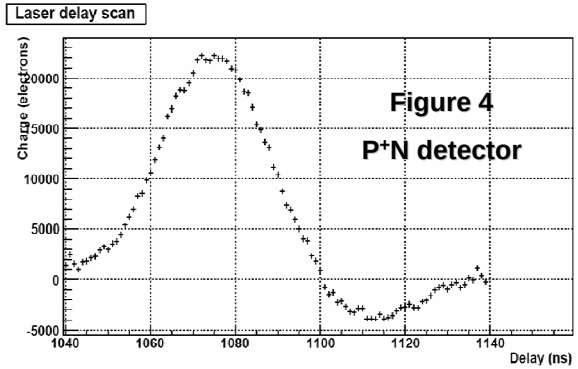
Measurements with non-irradiated detectors

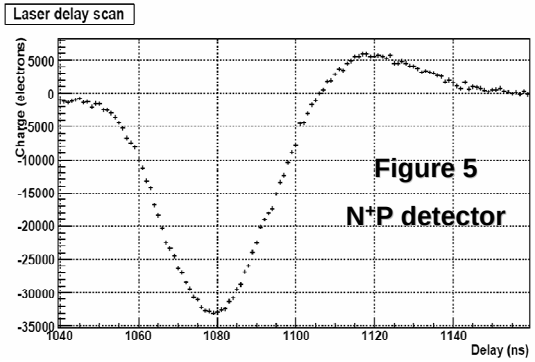
- Carried out with both non-irradiated **P⁺N** and **N⁺P detectors.**
- At T = 20 ºC with both laser setup and radioactive source setup.
- Calibration data is ok at T = 20 ºC: we calculate the ADC counts/electrons rate for each input channel (figure 1).
- Measurements with β source (^{90}Sr) as expected.
  - We can calculate the noise from the signal spectum (figure 2): σ ~ 1200 electrons.
  - Also the charge corresponding to a mip from the signal spectrum with a time cut (figure 3): peak of the distribution 26940 electrons
  - SNR as mip charge divided by noise: ~ 22.
- Measurements with laser setup as expected as well.
  - We can obtain the pulse shape reconstruction (figure 4 and figure 5).
  - Also the spectrum of the signal acquired.







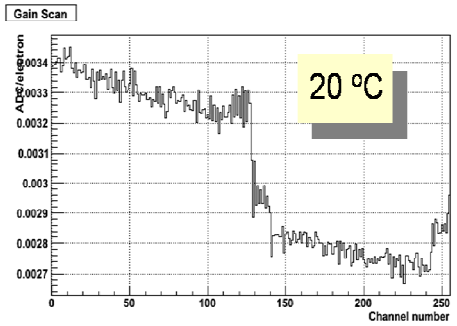


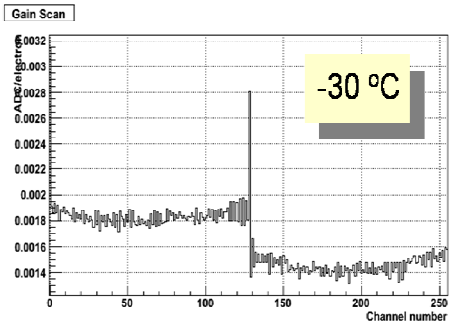


Measurements with irradiated detectors (I)

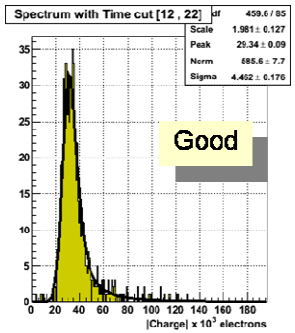
- Carried out with both irradiated **P⁺N** and **N⁺P detectors.**
- We operate the system inside a fridge (DB) @ -30 ºC. With both laser setup and radioactive source setup.
- Due to a input common mode range limitation in the DB buffer at low T: gain changes are not tracked by calibration.
- To overcome this limitation:
  - We used calibration data at 20 ºC.
  - We calculated a gain correction factor with a non-irradiated detector and the source:

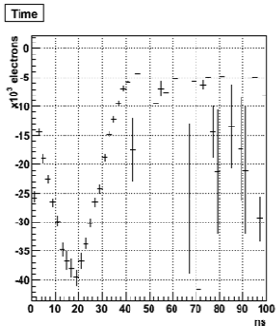
$$Rcal = Q_{outside}/Q_{inside}$$



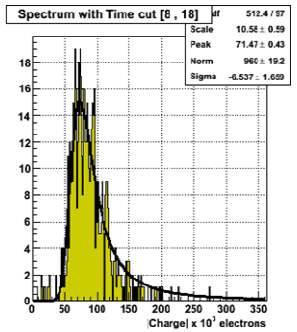


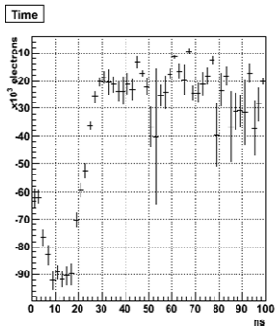
β source @ outside/cal. out.



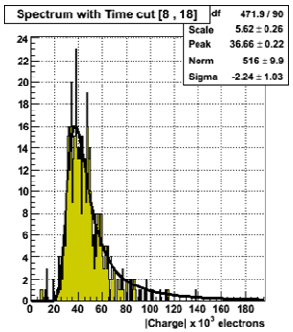


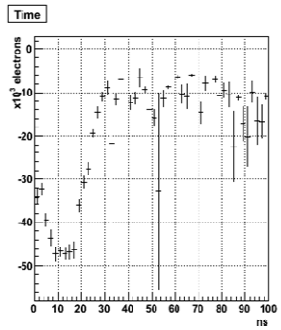
β source @ inside/cal. in.





β source @ inside/cal. out.





Measurements with irradiated detectors (II)

Non-irradiated, 300 mm thick, n-in-p FZ

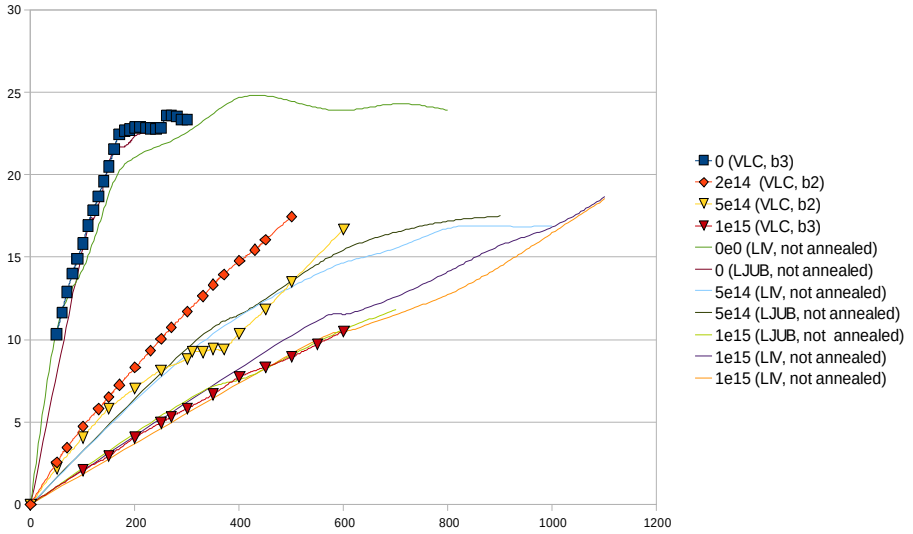
Temperature	Signal (ADC)	Gain (Unbonded)	Gain (Bonded)	Signal (Unbonded gain)	Signal (Bonded gain)
+ 20 C	206	118 e-/ADC	141 e-/ADC	24200	29000
– 20 C	230	102 e-/ADC	119 e-/ADC	23500	27400

- Finally, we have increased the common mode limit of the DB buffer by changing the buffer supply level from 3.3 V to 5 V.
- With this modification:
  - Calibration data is ok at -30 ºC.
  - Gain changes with T are accurately tracked by calibration.
  - There is no need to use a gain correction factor.
- Therefore, measurements at low T with irradiated sensors can be carried out without any problem.

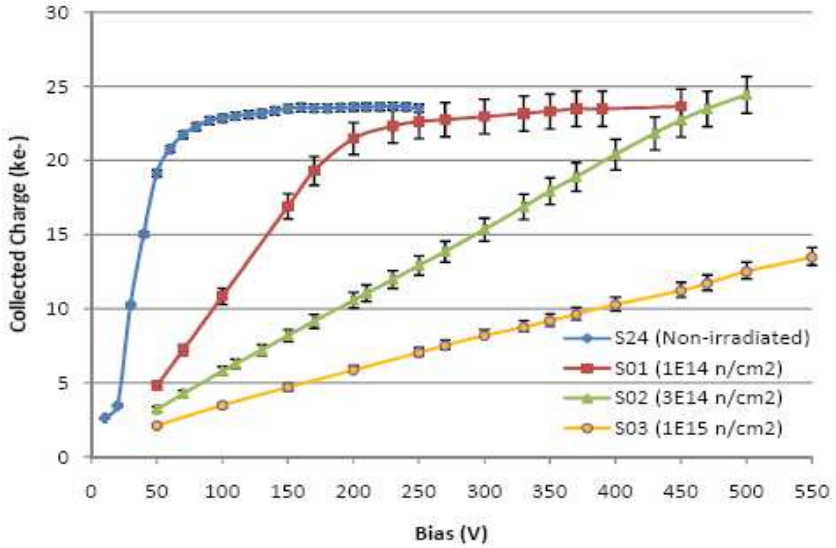
Charge collection measurements

- We measure on ADCs and we use the calibration data to obtain the charge in electrons: Q_{cal}
- We scan the voltages with laser and measure with β source for a few voltages (low activity source)
  - We compute $R_{src} = Q_{source}/Q_{laser}$
- We *normalize* so that the peak of the source in non-irradiated sensors is at 24000 electrons.
  - R_{24ke}
- All in all, for the laser data:

$$Q = R_{24ke} \times R_{src} \times Q_{cal}$$



Measurements of collected charge carried out with ALIBAVA system in Valencia. ATLAS07 sensors irradiated with neutrons. Presented by C. Lacasta in ATLAS Tracker Upgrade Workshop, NIIKHEF,November 2008.



Measurements of collected charge carried out with ALIBAVA system in Valencia. 300 μm n-on-n FZ sensors irradiated with neutrons. Presented by U. Soldevilla in 14th RD50 Workshop, Freiburg,June 2009.

Summary

- The readout system has been developed and is fully operational.
- The system can operate with different types and different sizes of microstrip detectors:
  - n-type.
  - p-type.
  - Irradiated and non-irradiated.
  - Up to 256 input channels.
  - Two flavours of detector boards to accommodate detectors of different sizes (1 cm^2 or 3 cm^2).
- The system is designed to work with a radioactive source setup and laser setup:
  - Useful for comparing results with the same detector.
  - Data can be acquired faster by combining a source setup and a laser setup
- The system has been tested with laser setup and a β source:
  - It works correctly: already used for carrying out measurements.
  - With p-type and n-type detectors.
  - SNR with the source is enough for irradiated and non-irradiated detectors.
  - Calibration factor had to be calculated for measurements at low T (-30 ºC) but this have been modified.
- Data acquired with the system can be easily processed using ROOT framework: some macros already developed.
- The system has been distributed among RD50 Collaboration members and other research groups.
- Future work:
  - Upgrade of the system for testbeam acquisition by synchronizing various ALIBAVAs.

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Instituto de Física Corpuscular (IFIC), Universidad de Valencia-CSIC,Valencia, Spain.

Backup: correction factors

- Correction factors:
  - Comparison between collected charge by radiation source and laser

$$Rsrc = \frac{\text{Collected Charge (source setup)}}{\text{Collected Charge (laser setup)}}$$

(Non-irradiated sensor)

  - Normalization of the radioactive source's peak at 24.000 electrons

$$R_{24} = \frac{24}{Q_{mean}\ \text{(source setup)}}$$

(Non-irradiated sensor)

  - Temperature dependence: Use calibration at 20ºC and gain correction factor (only applied to irradiated sensors)

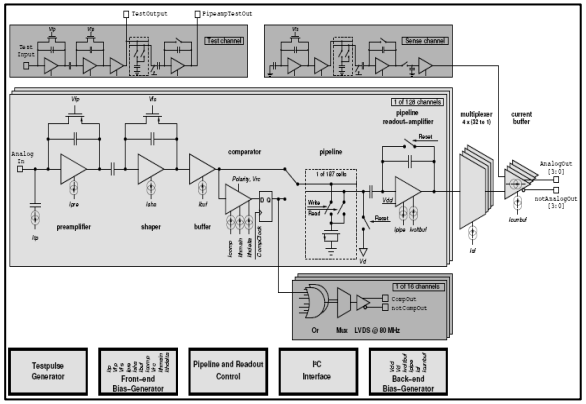
$$R_{cal} = \frac{Q_{outside\ (source\ setup)}}{Q_{inside\ (source\ setup)}}$$

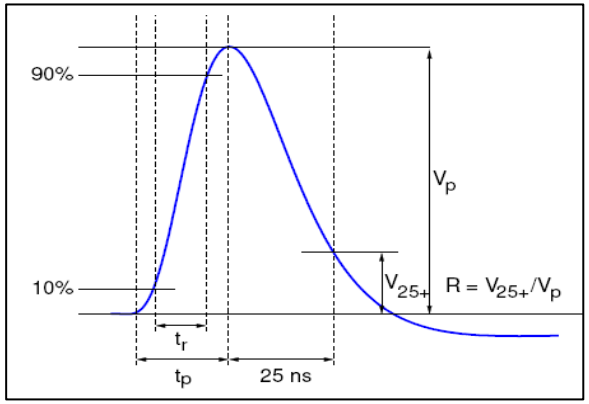
(Non-irradiated sensor)

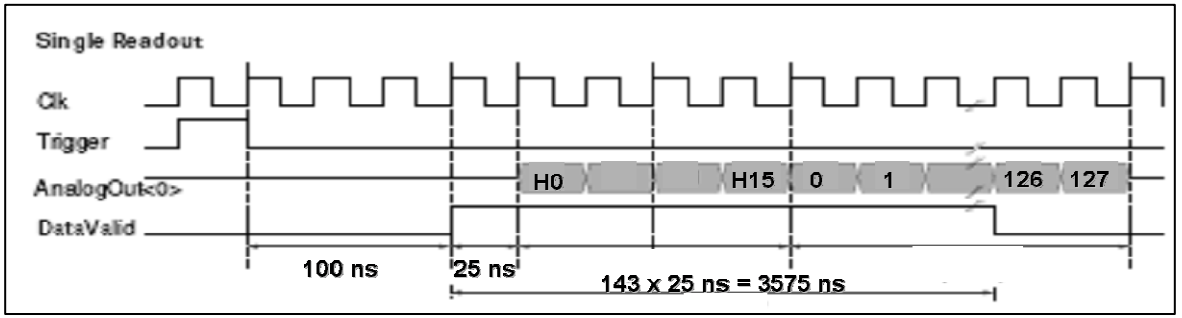
- For laser data with irradiated detectors: $\mathbf{Q_{corrected} = R_{24} \times Rcal \times Rsrc \times Q_{cal}}$
  - Q_{cal} is the collected charge in electrons with the calibration (ADC/electrons conversion)

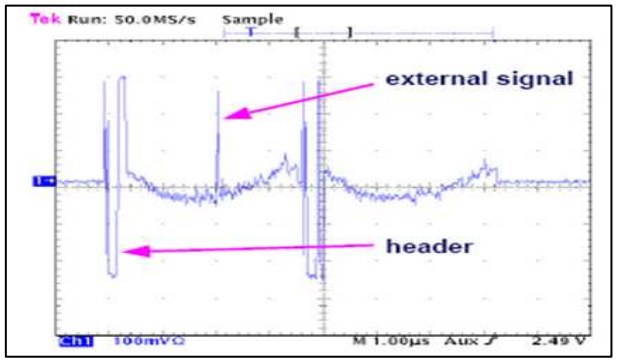
Backup: Beetle chip

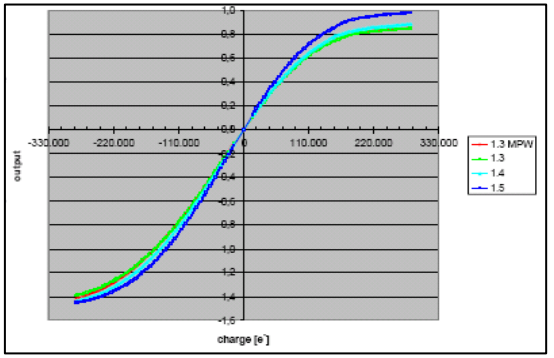
- Readout chip developed at ***ASIC laboratory of the University of Heildelberg.***
- 128 input channels:
  - Front-end (preamplifier + shaper). V_p = kQ. T_p ~ 25 ns. Total pulse length about 65-70 ns.
  - Front-end output signal is sampled into the analogue pipeline (128x187 cells) with the frequency of the Beetle chip clock (40 MHz).
  - Analogue pipeline programmable latency fixed to 128 CLK cycles (3.2 μs).
- Slow Control (I2C) signals for configuration.
- Fast Control (LVDS) signals: Trigger, Clock, TestPulse and Reset.
- Output format:
  - Analogue output format: single readout onto one port.
  - Readout: 16 bits header + 128 analogue multiplexed channels.
  - Channel width of 25 ns (40 MHz clock).
  - DataValid (LVDS) signal for readout detection.
  - Output dynamic range: linear up to ~ ±110000 e^-.





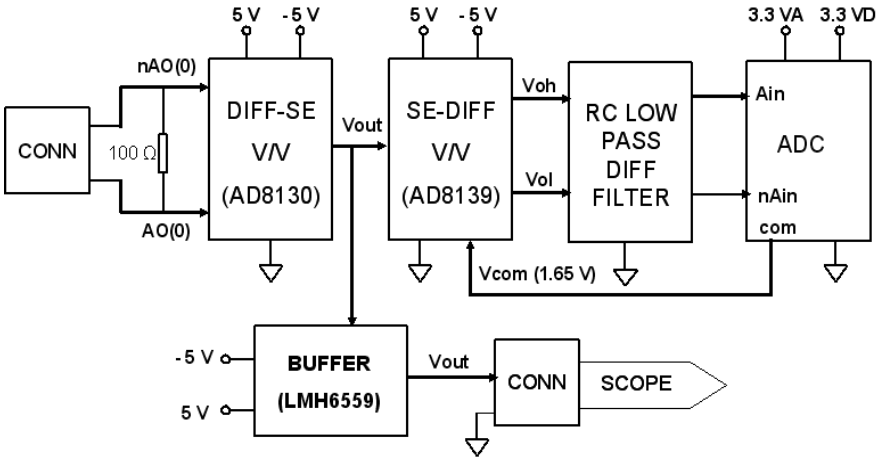


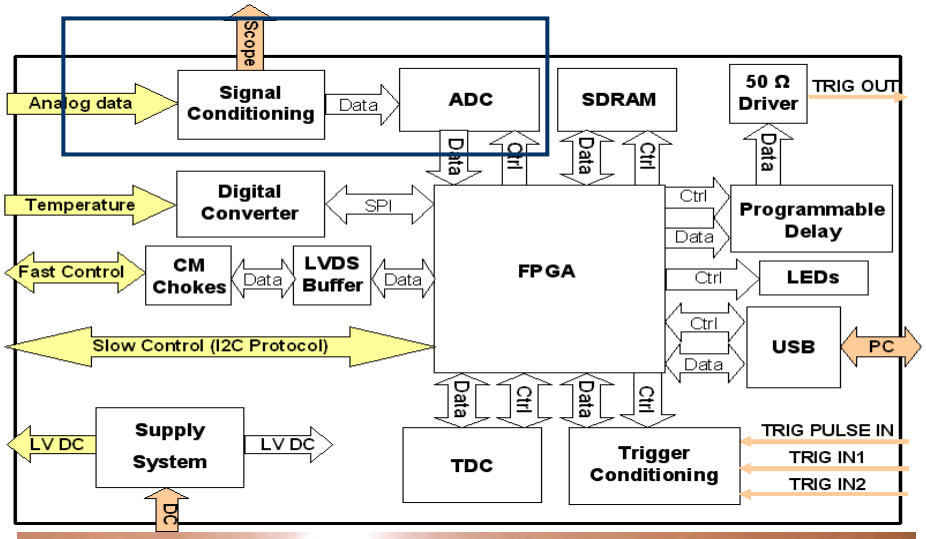


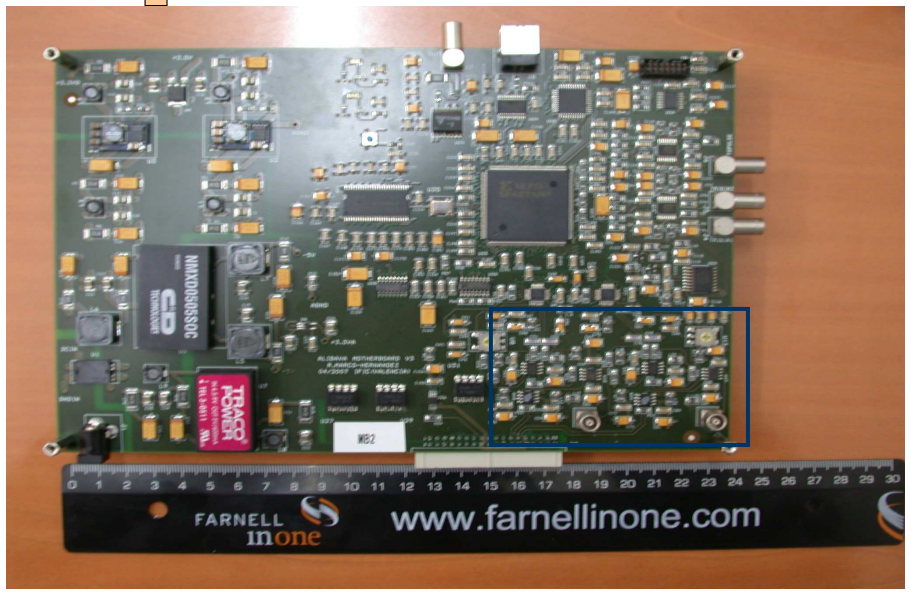


Backup: Mother board (I)

- Signal conditioning block transforms the differential voltage analogue input signal from each Beetle to:
  - Drive an oscilloscope: single ended signal.
  - Drive ADC: differential input shifted signal.
- ADC (one for each Beetle):
  - 10 bit flash type with a sample rate of 40 MHz (MAX1448).
  - Nominal resolution of 1 mV (output signed code, 9 bits plus 1 sign bit).
  - Dynamic range will be ±1024 mV.

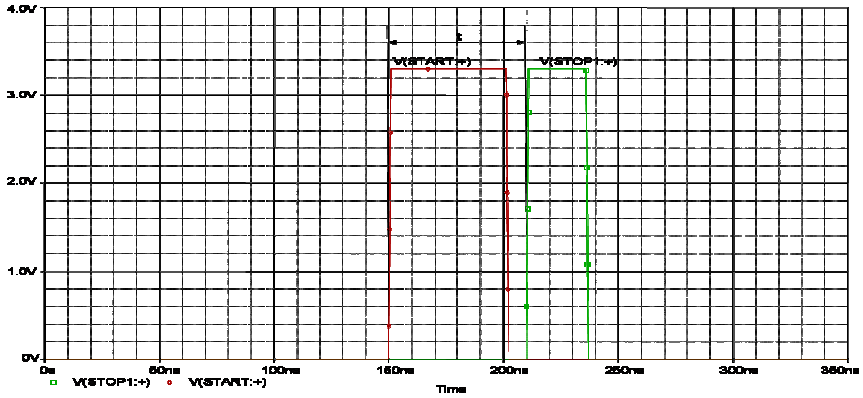


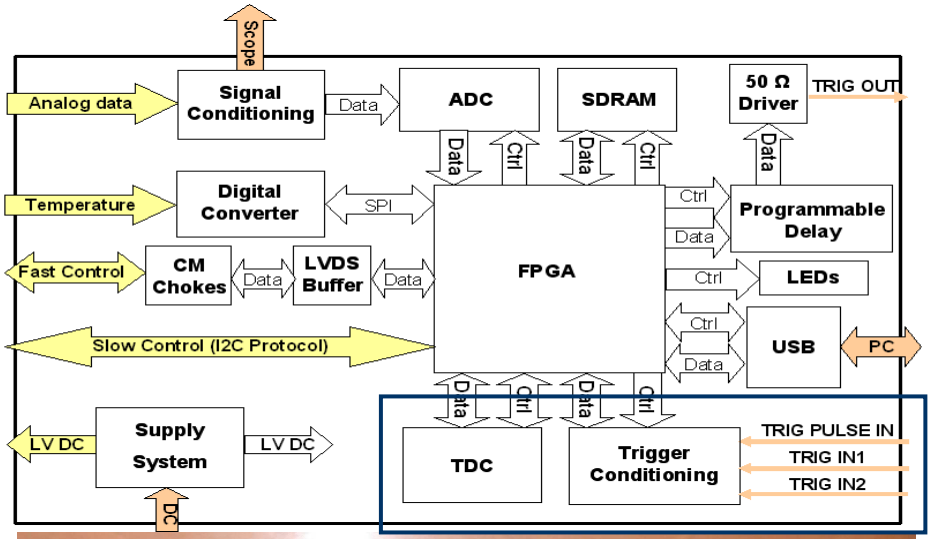


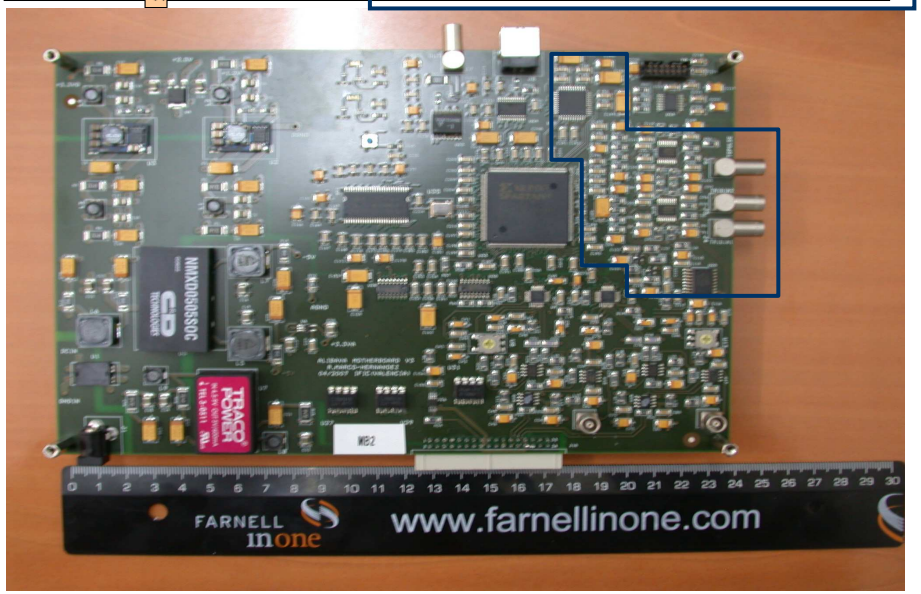


Backup: Mother board (II)

- In case of radioactive source setup for obtaining a time stamp of each trigger.
- Trigger conditioning:
  - Leading-edge discrimination for two photomultiplier analogue input signals.
  - Level conversion for an auxiliary signal (current or voltage).
  - Two dual LVPECL high speed comparators (MAX9601).
  - Four programmable voltage thresholds: generated with a quad 12 bits DAC (DAC7614).
- TDC: measurement of t between input trigger and a reference signal.
  - A TDC integrated circuit (TDC-GP1).
  - Nominal resolution: 600 ps.
  - 100 ns dynamic range.

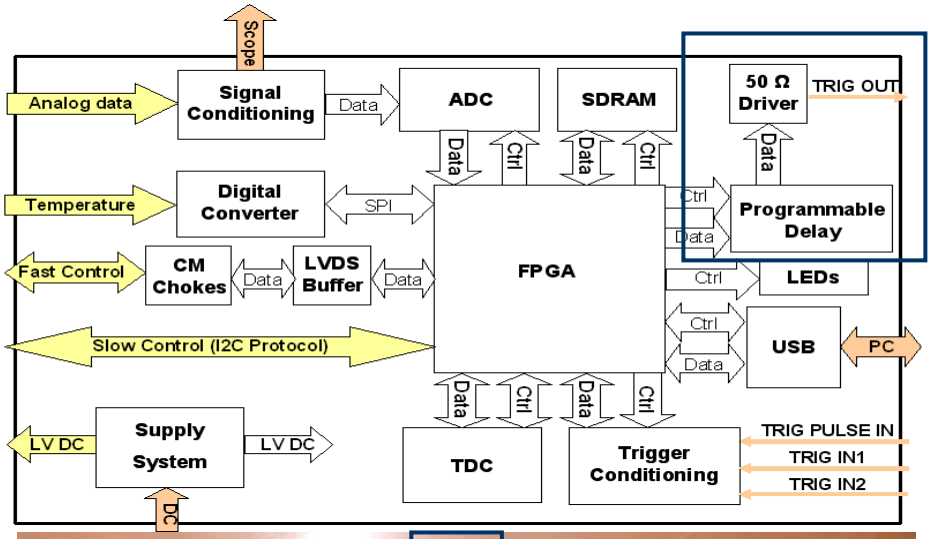


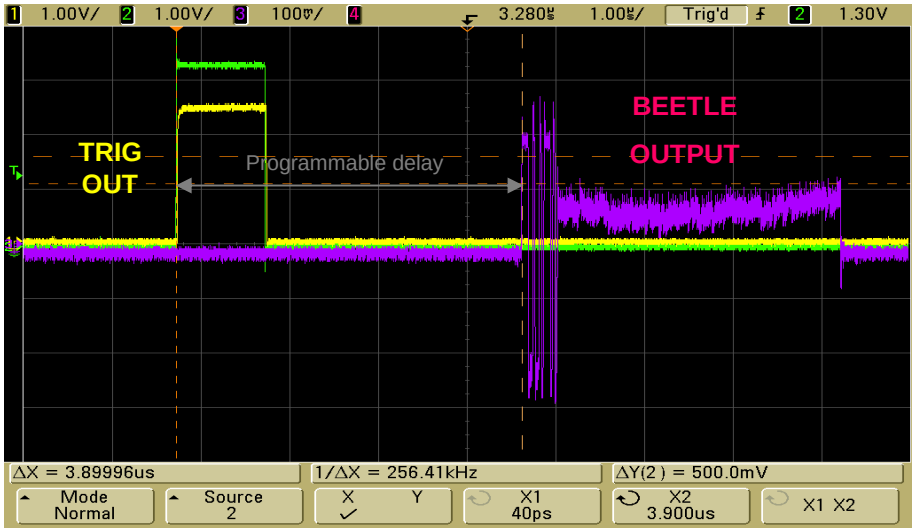


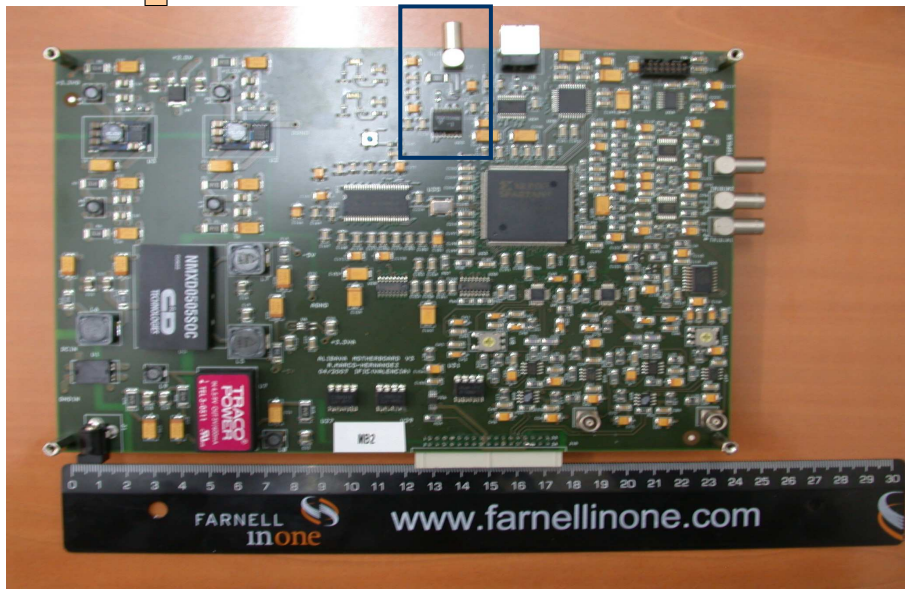


Backup: Mother board (III)

- In case of laser setup.
- A synchronised trigger signal (TRIG OUT) will be generated to drive a laser source to reconstruct the Beetle front-end pulse shape.
- Programmable delay circuit (3D7428):
  - Resolution: 1 ns.
  - Range: up to 255 ns.
  - Programmed by FPGA by serial interface.
- Following this block a 50 Ω driver will be incorporated for driving a pulse generator input.







Backup: Mother board (IV)

- FPGA hardware: Xilinx Spartan-3 (XS3400-PQ208) clocked at 40 MHz.
- Custom FPGA logic blocks:
  - Radioactive source: the DAC CONTROL, TRIGGER IN and TDC CONTROL for processing the trigger inputs and obtaining a time stamp of each trigger.
  - Laser setup: the TRIGGER OUT block for generating the output trigger signal and controlling the programmable delay circuit.
  - ADC CONTROL: for reading out the digitized data frames from input DataValid (fast control) signal leading edge.
  - BEETLE FAST CONTROL: generation of fast control signals (Clk, Trigger, Testpulse and Reset).
  - BEETLE SLOW CONTROL: I2C master controller.
  - SDRAM CONTROL and USB CONTROL: for external interface.
- A CFSM for controlling the custom blocks: implemented with an embedded system.
  - Soft processor: Microblaze (32 bits RISC) at 40 MHz.
  - SDRAM controller included as standard peripheral for the Microblaze.
  - ARBITRER: custom block of registers for communication between the embedded processor and the custom logic blocks.