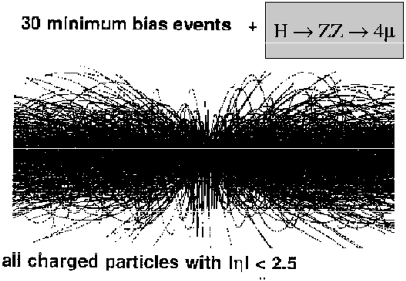
The Fast Tracker Architecture for the LHC baseline luminosity

G. Volpi for the FTK Collaboration

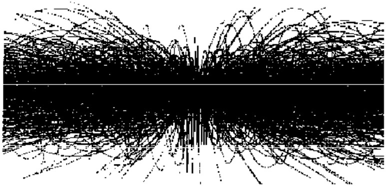
17/07/2009 - EPS 2009 - Kraków

Online tracking work

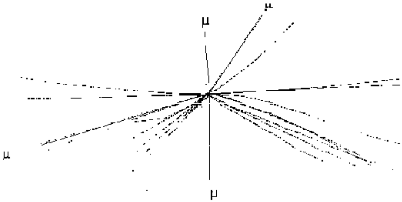


Online tracking work

30 minimum bias events + $H \rightarrow ZZ \rightarrow 4\mu$

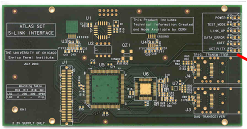


all charged particles with $|\eta| < 2.5$

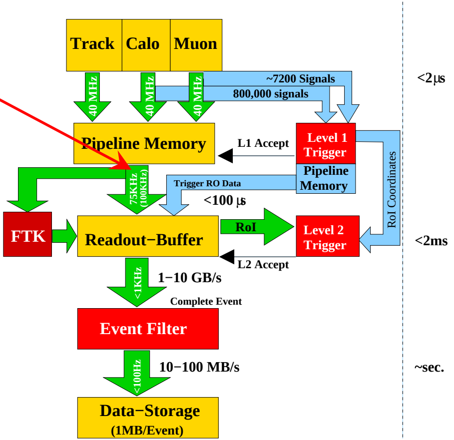


reconstructed tracks with $p_t > 2.0$ GeV

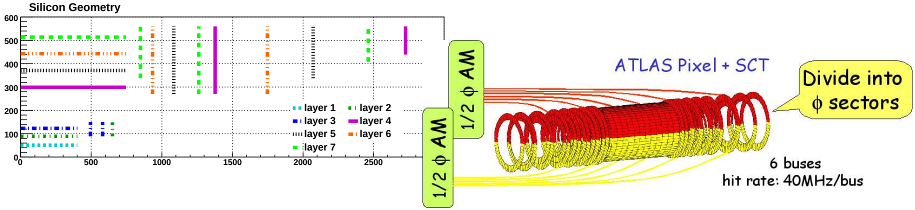
Connection with the ATLAS DAQ



- The Fast Track processor receives data from the ROD
- ROD output is duplicated by a dual output board
- FTK operates in parallel with the silicon tracker readout following each Level-1 trigger, reconstructing the tracks for use at the beginning of Level-2 trigger processing

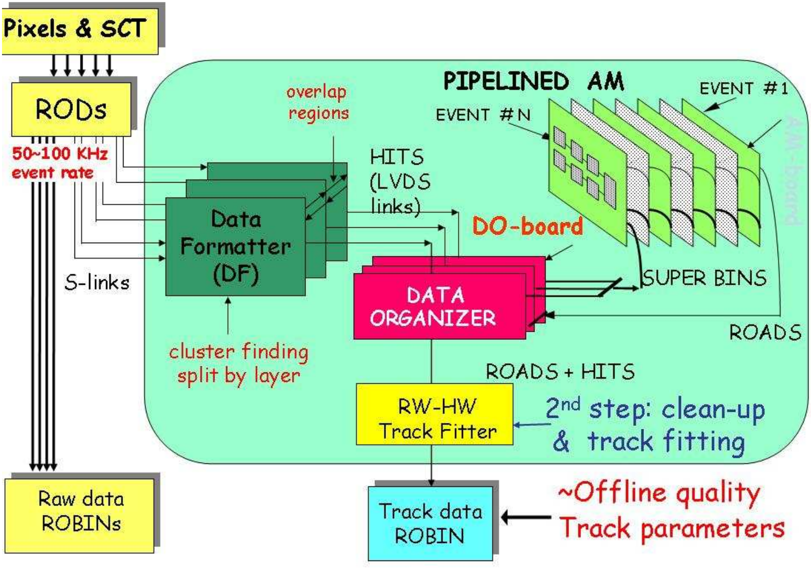


Detector Read-out



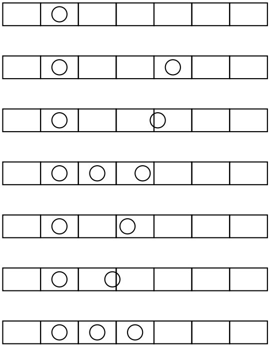
- FTK will use all the silicon layers: 3 pixel planes + 8 SCT axial and stereo planes, using barrel and end-cap regions:
  - 11 layers used to do pattern matching
  - 14 input coordinates are used to evaluate the track parameters
- Detector data flow divided in 8 ϕ-regions
  - FTK processors replicate and work in parallel in each region
  - The regions are defined with a generous overlap to avoid inefficiencies at the edges

FTK internal structure



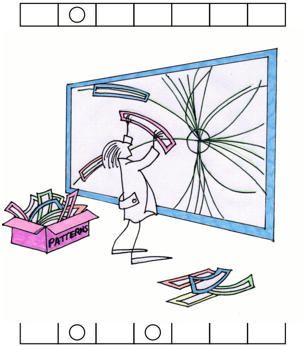
Pattern recognition with AM

- Pattern recognition is CPU demanding in crowded events
- Task simplified using a coarse segmentation of the silicon detector (a few mm): adjacent strips (or pixels) grouped in Super-Strips (SS)
- The track search happens during detector Read-out without the need of additional time
  - Precalculated using MC simulation or training data samples to create the Pattern Bank (PB)
  - Searched using AM to exploit the maximum parallelism



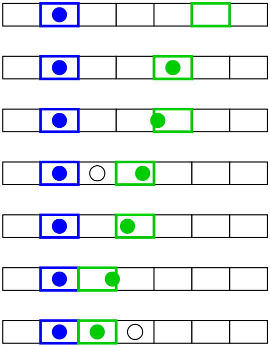
Pattern recognition with AM

- Pattern recognition is CPU demanding in crowded events
- Task simplified using a coarse segmentation of the silicon detector (a few mm): adjacent strips (or pixels) grouped in Super-Strips (SS)
- The track search happens during detector Read-out without the need of additional time
  - Precalculated using MC simulation or training data samples to create the Pattern Bank (PB)
  - Searched using AM to exploit the maximum parallelism



Pattern recognition with AM

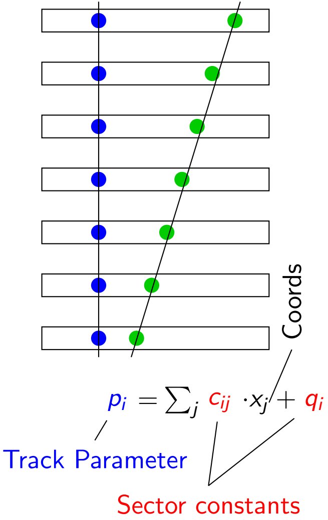
- Pattern recognition is CPU demanding in crowded events
- Task simplified using a coarse segmentation of the silicon detector (a few mm): adjacent strips (or pixels) grouped in Super-Strips (SS)
- The track search happens during detector Read-out without the need of additional time
  - Precalculated using MC simulation or training data samples to create the Pattern Bank (PB)
  - Searched using AM to exploit the maximum parallelism



- Only hits within the roads go to the next step
- Also roads with one missing layers are accepted (☐)

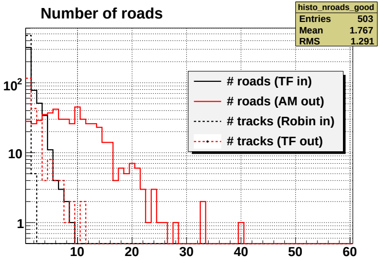
Fitting with linear constraints

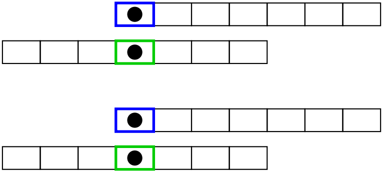
- Fit limited to hits matching a road in the PB
- Track fitting problem is reduced to a linear problem: **scalar products**
  - Approximation valid grouping patterns in limited geometrical regions
  - Linear constraints between track' hits are evaluated to provide a track χ^2
  - Problem suitable for FPGA configured with DSPs
- In each road, all hit combinations are fit
- For each combination the 5 3D track parameters (Curvature, d_0, ..) and a quality parameter (χ^2) are calculated



Roads and tracks reduction algorithms

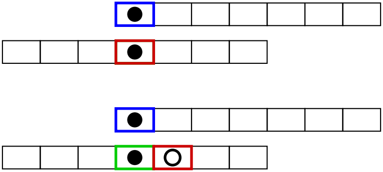
- Duplicated tracks (ghosts) are common problem for tracking algorithm
- In FTK the problem is increased by the overlap of the silicon modules
- Two type of ghosts: ghost roads, ghost tracks

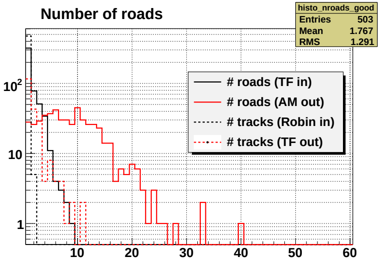




Roads and tracks reduction algorithms

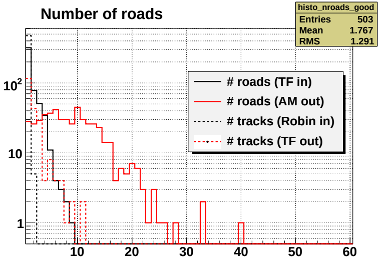
- Duplicated tracks (ghosts) are common problem for tracking algorithm
- In FTK the problem is increased by the overlap of the silicon modules
- Two type of ghosts: ghost roads, ghost tracks

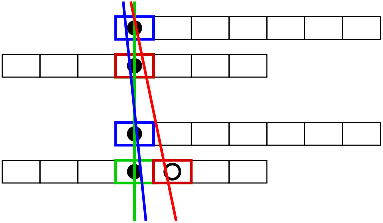




Roads and tracks reduction algorithms

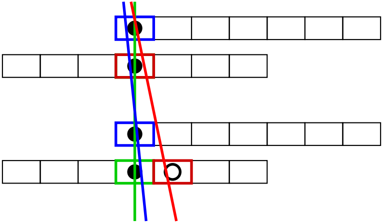
- Duplicated tracks (ghosts) are common problem for tracking algorithm
- In FTK the problem is increased by the overlap of the silicon modules
- Two type of ghosts: ghost roads, ghost tracks

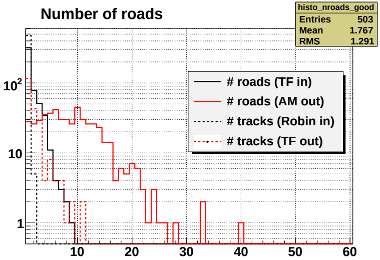




Roads and tracks reduction algorithms

- Duplicated tracks (ghosts) are common problem for tracking algorithm
- In FTK the problem is increased by the overlap of the silicon modules
- Two type of ghosts: ghost roads, ghost tracks

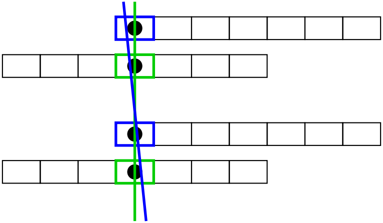


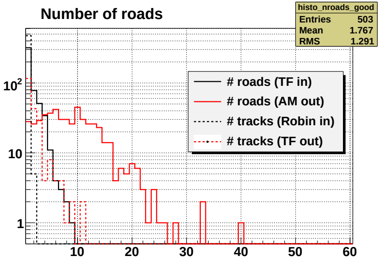


- Two logical steps:
  - Road-Warrior: to reject roads, before the fits

Roads and tracks reduction algorithms

- Duplicated tracks (ghosts) are common problem for tracking algorithm
- In FTK the problem is increased by the overlap of the silicon modules
- Two type of ghosts: ghost roads, ghost tracks

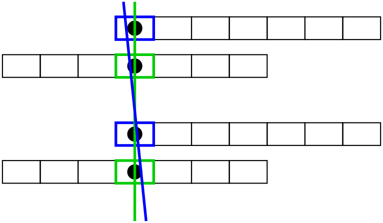


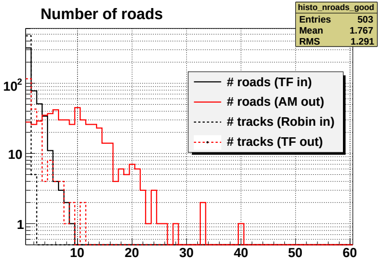


- Two logical steps:
  - Road-Warrior: to reject roads, before the fits

Roads and tracks reduction algorithms

- Duplicated tracks (ghosts) are common problem for tracking algorithm
- In FTK the problem is increased by the overlap of the silicon modules
- Two type of ghosts: ghost roads, ghost tracks

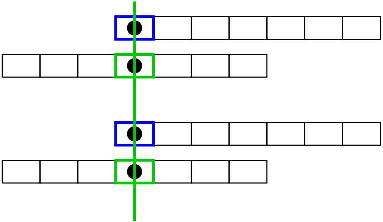


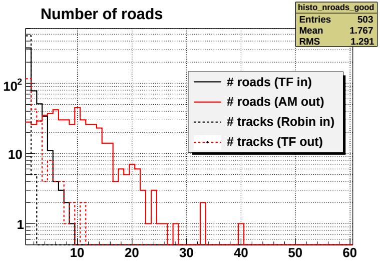


- Two logical steps:
  - Road-Warrior: to reject roads, before the fits
  - Hit-Warrior: to reduce tracks sharing similar hits after fitting

Roads and tracks reduction algorithms

- Duplicated tracks (ghosts) are common problem for tracking algorithm
- In FTK the problem is increased by the overlap of the silicon modules
- Two type of ghosts: ghost roads, ghost tracks

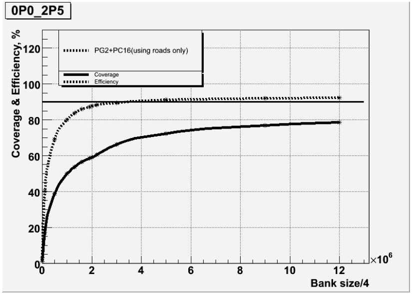




- Two logical steps:
  - Road-Warrior: to reject roads, before the fits
  - Hit-Warrior: to reduce tracks sharing similar hits after fitting

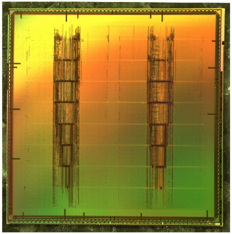
Pattern bank generation

- The size of the pattern bank greatly impacts the size and cost of the entire system
- The PB size is the leading factor on the track reconstruction efficiency
- For a PB we define two factors:
    - Coverage: the probability for a complete track to have a pattern. Geometrical parameter
    - Efficiency: the probability to be in a complete or an incomplete pattern

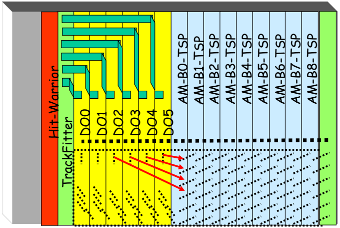


- Efficiency rises quickly to 90%
- From other considerations PB with $\sim 60 \times 10^6$ patterns are being considered.

The AM Chip and the crate structure



Current chip used at CDF: 0.18 μm custom cells, with 2500 pattern/chip. *IEEE Trans.Nucl. Vol. 53 Page(s):2428 - 2433*



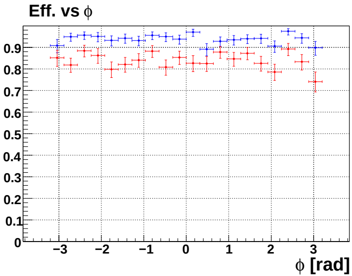
- The AM chip under consideration:
  - Using standard cells with $90\text{nm} \rightarrow 10000\text{pattern/chip}$
  - Using custom cells gives a factor 2
  - If the pattern banks are very large we could use 65 nm.

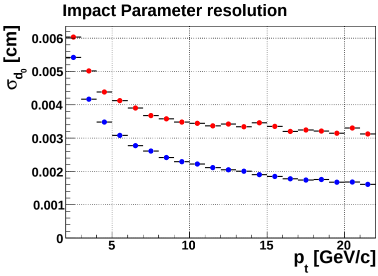
- Each crate will have the logic to fit one region
- The Pattern-Bank is split into several boards
- Track-fitter based on FPGA, similar hardware developed for CDF

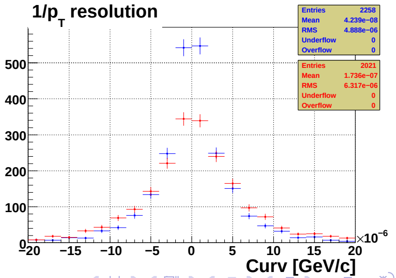
Performances in single muon events

- The efficiency is about 90%
- Resolution is comparable with the offline

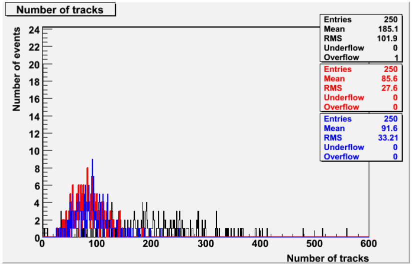
Parameter	$\sigma(FTK)$	$\sigma(\mathrm{OFF})$
$1/(2p_T)$ [c/GeV]	$7.4 \cdot 10^{-3}$	$6.6 \cdot 10^{-3}$
ϕ [rad]	$9.5 \cdot 10^{-4}$	$6.3 \cdot 10^{-4}$
d_0 [cm]	$5.3 \cdot 10^{-3}$	$3.3 \cdot 10^{-3}$
$\cot(\theta)$	$2.0 \cdot 10^{-3}$	$1.4 \cdot 10^{-3}$
z_0 [mm]	$2.1 \cdot 10^{-2}$	$1.9 \cdot 10^{-2}$

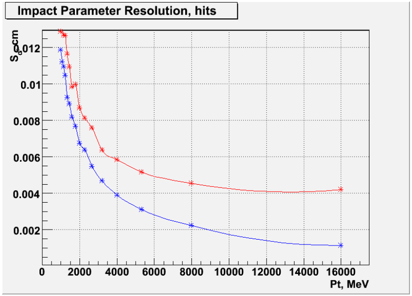


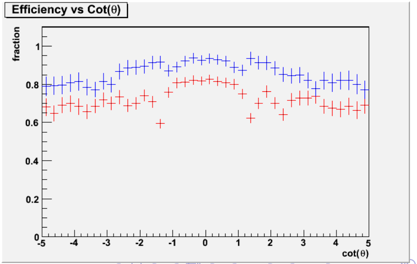




$WH \to b\bar{b}X@10^{34}\,\mathrm{cm}^{-1}\mathrm{s}^{-1}$ events



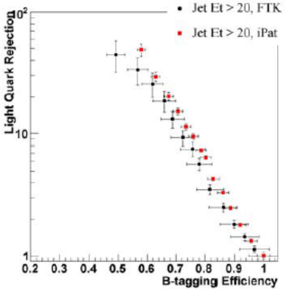


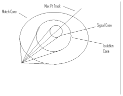


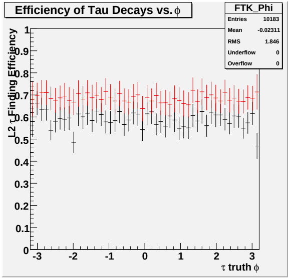
- Single tracks performances are stable also in Hi-lumi samples
  - Efficiency is a bit lower because quality cut is more tight
- Fake rate under control, comparable with the off-line

FTK tracks use (preliminary)

- The use of the FTK or offline tracks as input to b-tagging algorithm is comparable.
  - The time saved in track finding/fitting can be used for more sophisticated b-tagging algorithms







- Effect on other physics object under study:
  - Rare decay of b-hadrons, as support of muon triggers

    Trans.Nucl.Sci.55:145-150,2008
  - Identification of tau using cone algorithm

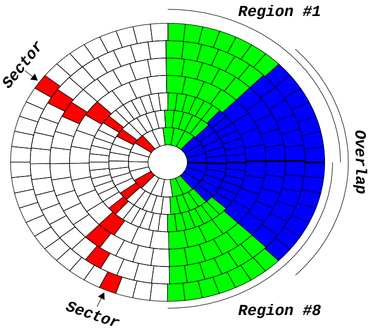
Conclusions

- FTK can provide global track reconstruction for every level-1 trigger
- The rapid execution time will provide a complete 3D track list at the beginning of level-2 processing
- The integration with current ATLAS DAQ is “easy”
- Single track quality is comparable with the off-line algorithms
    - It opens the possibility to have more refined L2 algorithms, using more information than a single Region of Interest
- Schedule for the project is challenging:
    - TDR ready for the fall
    - First prototypes of the board in the following year.
    - Completion of the system prior to the LHC Phase I shutdown
- The AM architecture is ready and scalable:
    - Tuning studies are on-going
    - Different options are ready if larger pattern banks are needed

Backup slides

Regions and sectors

- Regions are contiguous geometrical regions
- Two neighboring regions share few modules to limit inefficiency at the borders
- A sector is sequence of silicon modules, one per plane
- Each sector has its set of fit constants



Number of fits

- In $WH@10^{-34}$ events number of roads and fits per event is high:
  - $\langle \# \, roads \rangle = 40 \times 10^3$
  - $\langle \# \, fits \rangle = 2 \times 10^6$
- Number of road doesn't use all the RW stages
- Number of fits affordable (1 fit per ns)
  - Fit reduction improving RW efficiency
  - Decrease the SS size
  - Increase the number of FPGAs